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**Multimedia ICs**

# 16-bit stereo D / A converter for audio applications

## BU9480F

The BU9480F is a 16-bit stereo D / A converter designed for audio applications, and has an internal 2 × oversampling circuit.

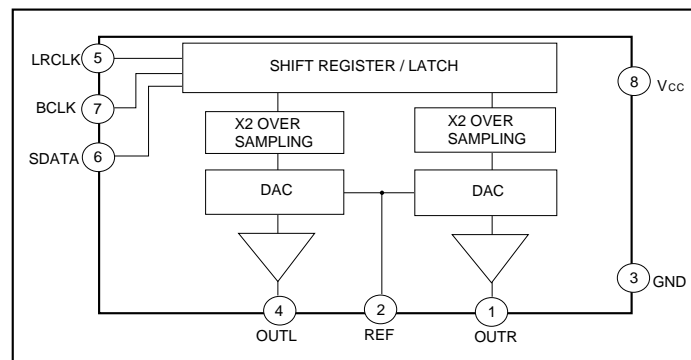
●Applications

16-bit stereo D / A converter for audio applications

●Features

- 1) 3.0 to 5.5V operating voltage.
- 2) Low current consumption because of the CMOS process.
- 3) Resistor strings method used.
- 4) 2-channel common phase output.
- 5) Internal 2 × oversampling interpolator.
- 6) 8 - pin plastic package.
- 7) Supports 4fs. (200kHz operation)

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function	I / O	Voltage
1	R <sub>OUT</sub>	Right channel analog signal output	Low-impedance output	1 / 2V <sub>CC</sub>
2	REF	Connects the DA ref. voltage pin and ground	High-impedance input	1 / 2V <sub>CC</sub>
3	GND	Ground	—	—
4	L <sub>OUT</sub>	Left channel analog signal output	Low-impedance output	1 / 2V <sub>CC</sub>
5	LRCK	The signal that distinguishes between left and right channels for serial data (left channel = high level, right channel = low level).	Logic input	—
6	SDAT	Serial data input Input with 2' compliment, MSB first.	Logic input	—
7	BCLK	Serial data shift clock input	Logic input	—
8	V <sub>CC</sub>	V <sub>CC</sub>	—	—

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**●Absolute maximum ratings (Ta = 25°C)**

Parameter	Symbol	Limits	Unit
Applied voltage	V <sub>DDMax.</sub>	7.0	V
Power dissipation	P <sub>d</sub>	450*	mW
Operating temperature	T <sub>opr</sub>	- 10 ~ + 70	°C
Storage temperature	T <sub>stg</sub>	- 55 ~ + 125	°C
Input voltage	T <sub>opt</sub>	- 0.3 ~ V <sub>DD</sub> + 0.3	V

\* When unmounted, reduced by 4.5mW for each increase in Ta of 1°C over 25°C.

**●Recommended operating conditions**

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub>	3.0 ~ 5.5	V
Input low level voltage	V <sub>IL</sub>	0.0 ~ 0.2 × V <sub>DD</sub>	V
Input high level voltage	V <sub>IH</sub>	0.8 × V <sub>DD</sub> ~ V <sub>DD</sub>	V

**●Electrical characteristics (unless otherwise noted, Ta = 25°C, V<sub>DD</sub> = + 5.0V)**
**Analog unit characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Current dissipation	I <sub>DD</sub>	—	3.6	6	mA	f = 1kHz, 0dB	Fig.6,7
Resolution	RES	—	—	16	BIT	—	Fig.6,7
Noise distortion 1	THD1	—	0.05	0.12	%	f = 1kHz, 0dB	Fig.6,7
Noise distortion 2	THD2	—	0.07	0.4	%	f = 1kHz, - 20dB	Fig.6,7
Full-scale output voltage	V <sub>FS</sub>	1.8	2	2.2	V <sub>P-P</sub>	—	Fig.6,7
Crosstalk	C.T	—	- 92	- 85	dB	Unmeasured channel output = 0 dB, f = 1kHz. DIN audio filter	Fig.6,7
S / N ratio	S / N	86	93	—	dB	DIN audio filter	Fig.6,7
Output pin load resistance	RL	10	—	—	kΩ	—	Fig.6,7

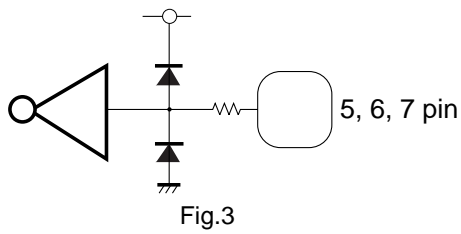
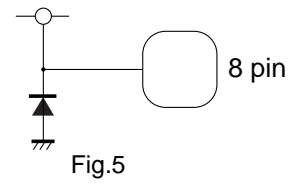
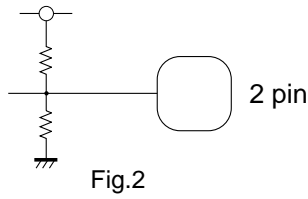
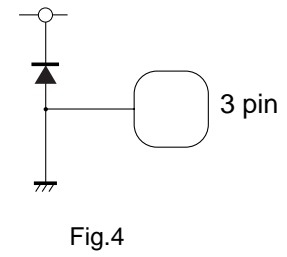
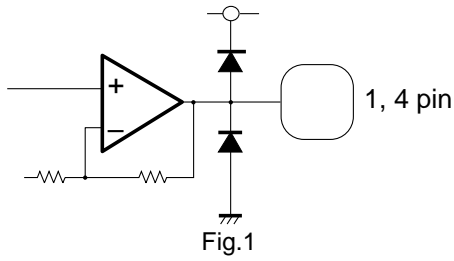
**Logic input characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Input high level voltage	V <sub>IH</sub>	0.7 × V <sub>DD</sub>	—	V <sub>DD</sub>	V	Pins 5,6 and 7	Fig.6,7
Input low level voltage	V <sub>IL</sub>	GND	—	0.3 × V <sub>DD</sub>	V	Pins 5,6 and 7	Fig.6,7
Leakage current, high level	I <sub>IH</sub>	—	—	- 10	μA	Pins 5,6 and 7 = V <sub>DD</sub>	Fig.6,7
Leakage current, low level	I <sub>IL</sub>	—	—	10	μA	Pins 5,6 and 7 = GND	Fig.6,7
DA conversion frequency	f <sub>SL</sub>	—	—	200	kHz	—	Fig.6,7
BCLK period	T <sub>BCLK</sub>	60	—	—	ns	—	Fig.6,7
SDAT.LRCK settling time	T <sub>ST</sub>	60	—	—	ns	—	Fig.6,7
SDAT.LRCK holding time	T <sub>HD</sub>	60	—	—	ns	—	Fig.6,7

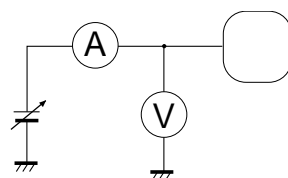
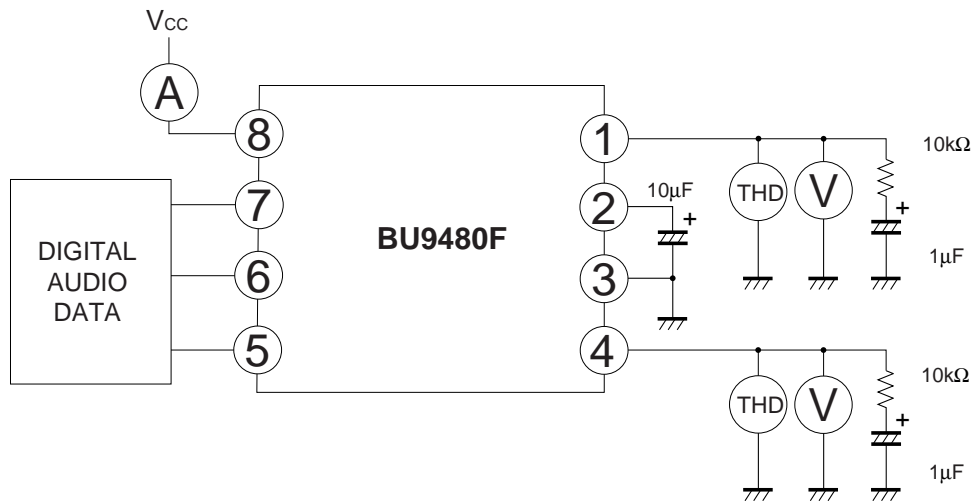
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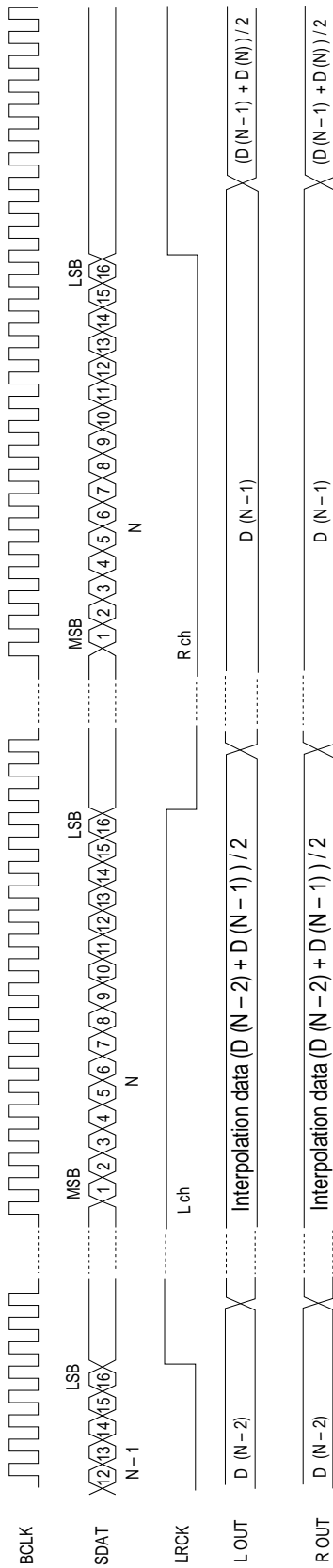
●Pin equivalent circuits



●Measurement circuits



● I / O signal timing chart



**Note:** Interpolation and original data output are timed respectively to the leading edge and leading edge of LRCK, and so LRCK should be set to a duty of 50%.

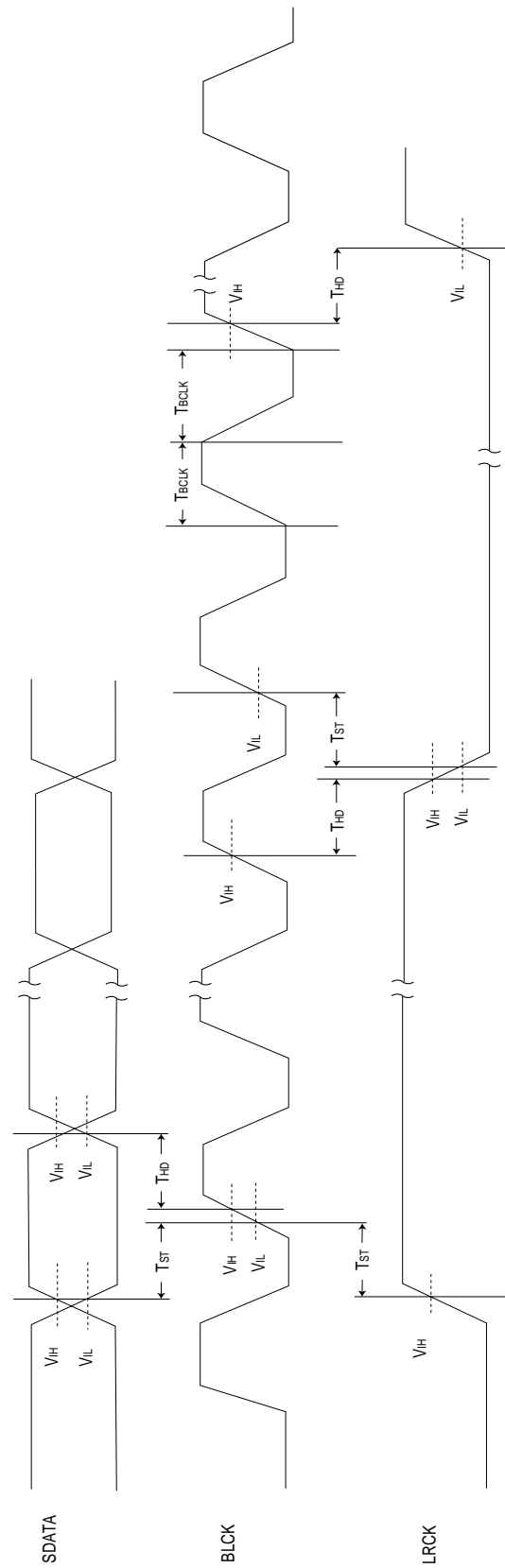
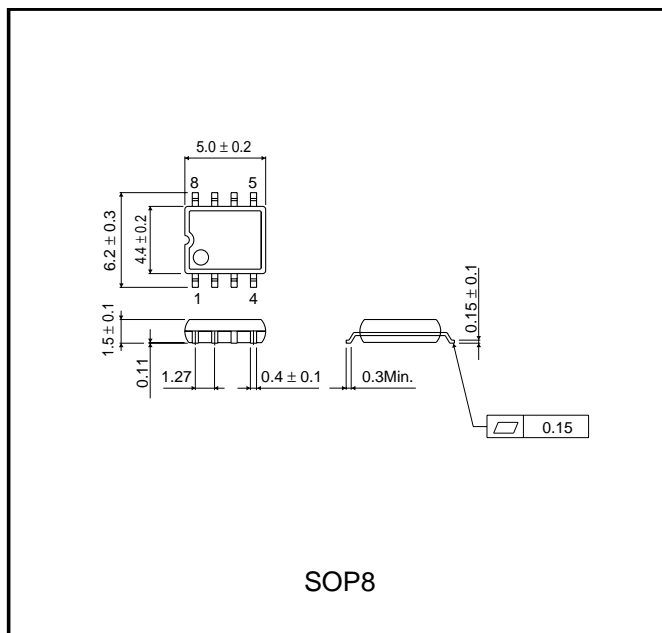


Fig. 8

●External dimensions (Units: mm)



## Appendix

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