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[NTB75N06LT4](#)

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NTP75N06L, NTB75N06L

Power MOSFET 75 Amps, 60 Volts, Logic Level

N-Channel TO-220 and D²PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb-Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 10\text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage	V_{GS}	± 20	Vdc
– Continuous	V_{GS}	± 15	
– Non-Repetitive ($t_p \leq 10\text{ ms}$)			
Drain Current	I_D	75	Adc
– Continuous @ $T_A = 25^\circ\text{C}$	I_D	50	
– Continuous @ $T_A = 100^\circ\text{C}$	I_{DM}	225	Apk
– Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	214	W
Derate above 25°C		1.4	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)		2.4	W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to $+175$	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50\text{ Vdc}$, $V_{GS} = 5.0\text{ Vdc}$, $L = 0.3\text{ mH}$ $I_{L(pk)} = 75\text{ A}$, $V_{DS} = 60\text{ Vdc}$)	E_{AS}	844	mJ
Thermal Resistance	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$
– Junction-to-Case	$R_{\theta JA}$	62.5	
– Junction-to-Ambient (Note 1)			
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in^2).

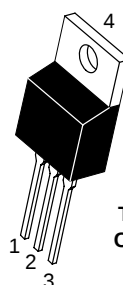
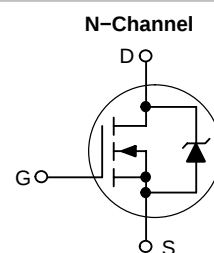


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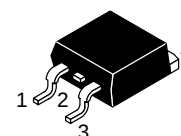
<http://onsemi.com>

75 AMPERES, 60 VOLTS

$R_{DS(on)} = 11\text{ m}\Omega$

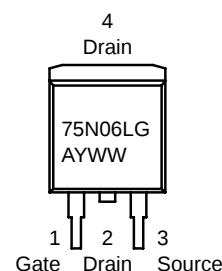
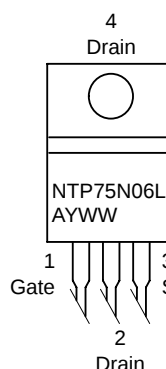


**TO-220AB
CASE 221A
STYLE 5**



**D²PAK
CASE 418B
STYLE 2**

MARKING DIAGRAMS & PIN ASSIGNMENTS



A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTP75N06L, NTB75N06L

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 2) (V _{GS} = 0 Vdc, I _D = 250 μ Adc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 –	72 74	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	10 100	μ Adc
Gate-Body Leakage Current (V _{GS} = $\pm$ 15 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	$\pm$ 100	nAdc

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage (Note 2) (V _{DS} = V _{GS} , I _D = 250 μ Adc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.58 6.0	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 2) (V _{GS} = 5.0 Vdc, I _D = 37.5 Adc)	R _{DS(on)}	–	9.0	11	m Ω
Static Drain-to-Source On-Voltage (Note 2) (V _{GS} = 5.0 Vdc, I _D = 75 Adc) (V _{GS} = 5.0 Vdc, I _D = 37.5 Adc, T _J = 150°C)	V _{DS(on)}	– –	0.75 0.61	0.99 –	Vdc
Forward Transconductance (Note 2) (V _{DS} = 15 Vdc, I _D = 37.5 Adc)	g _{FS}	–	55	–	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	3122	4370	pF
Output Capacitance		C _{oss}	–	1029	1440	
Transfer Capacitance		C _{rss}	–	276	390	

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 75 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω) (Note 2)	t _{d(on)}	–	22	32	ns
Rise Time		t _r	–	265	370	
Turn-Off Delay Time		t _{d(off)}	–	113	160	
Fall Time		t _f	–	170	240	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 75 Adc, V _{GS} = 5.0 Vdc) (Note 2)	Q _T	–	66	92	nC
		Q ₁	–	9.0	–	
		Q ₂	–	47	–	

SOURCE-DrAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 75 Adc, V _{GS} = 0 Vdc) (Note 2) (I _S = 75 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	– –	1.0 0.9	1.15 –	Vdc
Reverse Recovery Time	(I _S = 75 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/ μ s) (Note 2)	t _{rr}	–	70	–	ns
		t _a	–	43	–	
		t _b	–	27	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.16	–	μ C

2. Pulse Test: Pulse Width $\leq$ 300 μ s, Duty Cycle $\leq$ 2%.

3. Switching characteristics are independent of operating junction temperatures.

NTP75N06L, NTB75N06L

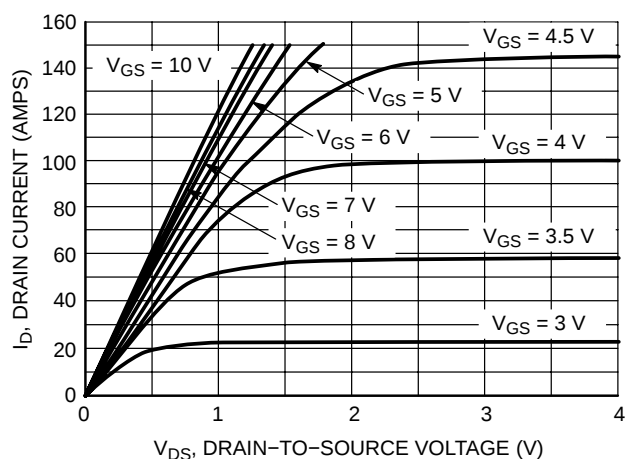


Figure 1. On-Region Characteristics

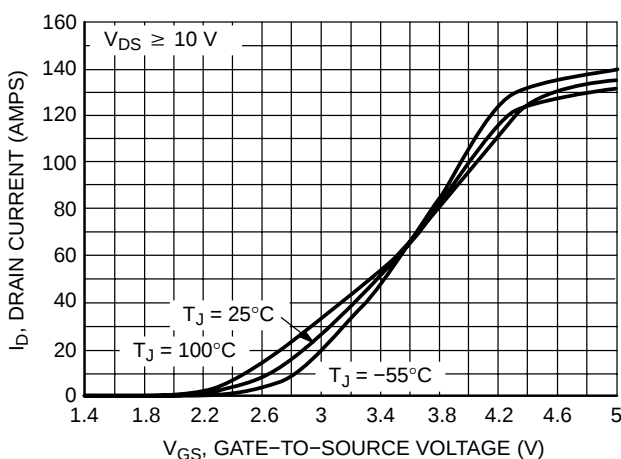


Figure 2. Transfer Characteristics

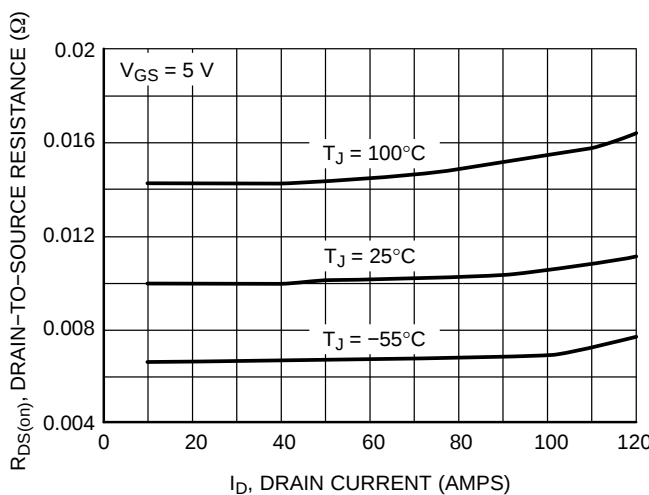


Figure 3. On-Resistance vs. Gate-to-Source Voltage

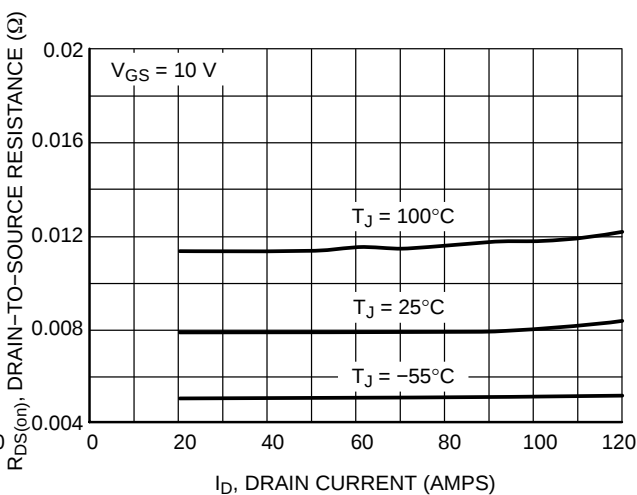


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

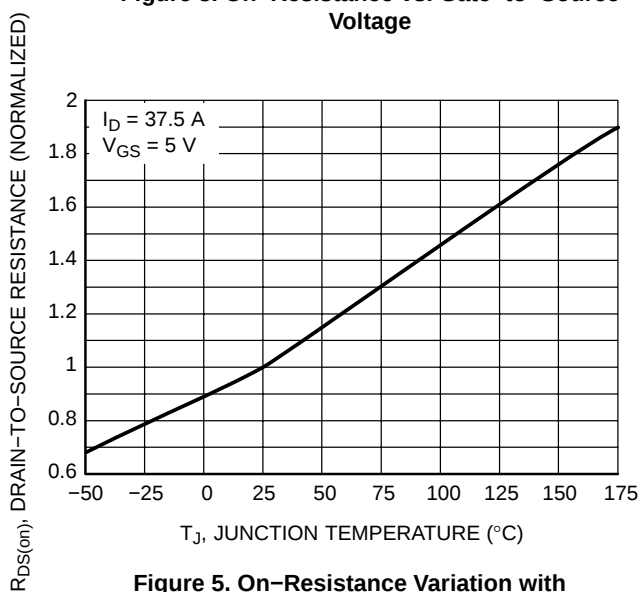


Figure 5. On-Resistance Variation with Temperature

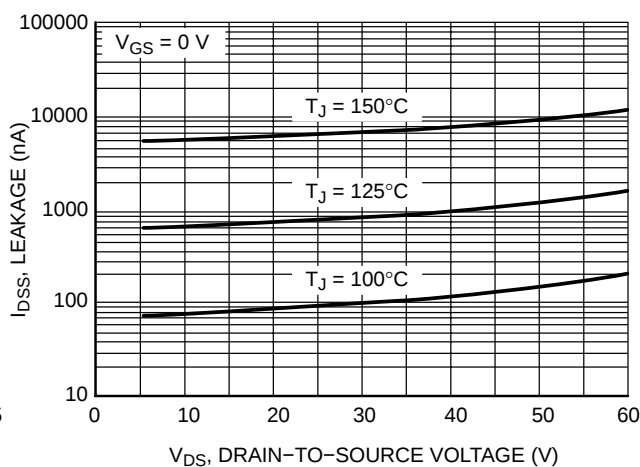


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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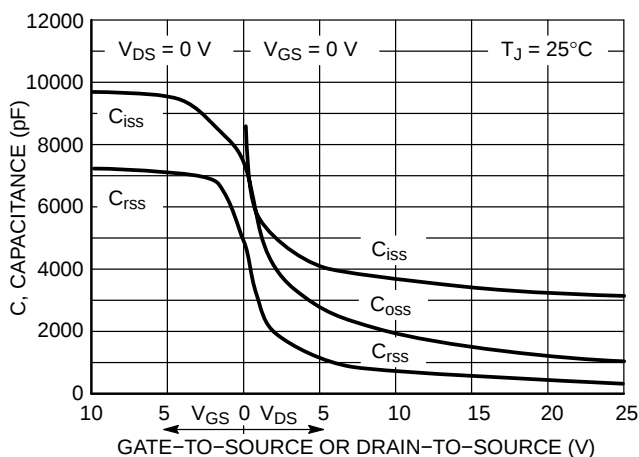


Figure 7. Capacitance Variation

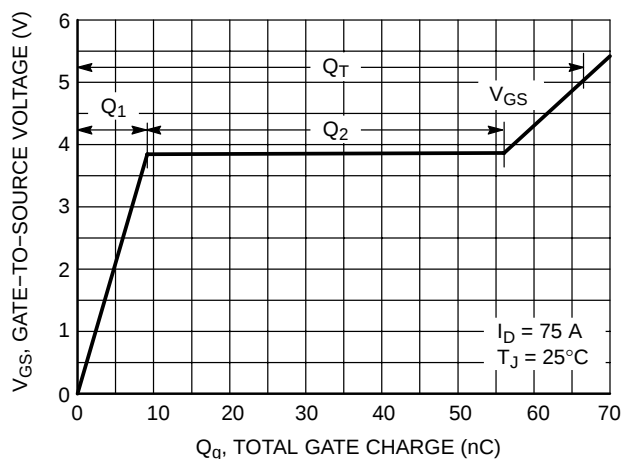


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

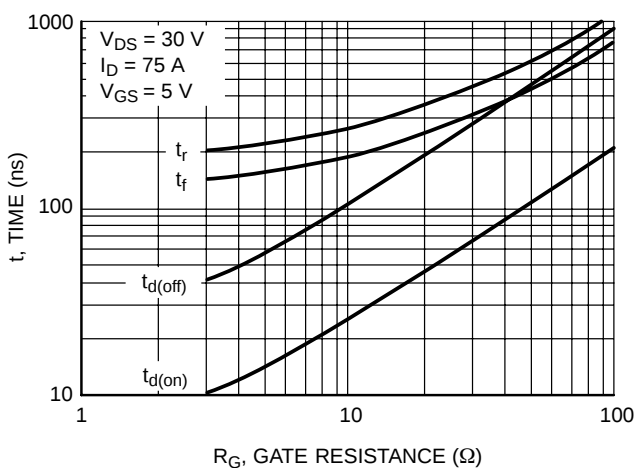


Figure 9. Resistive Switching Time Variations vs. Gate Resistance

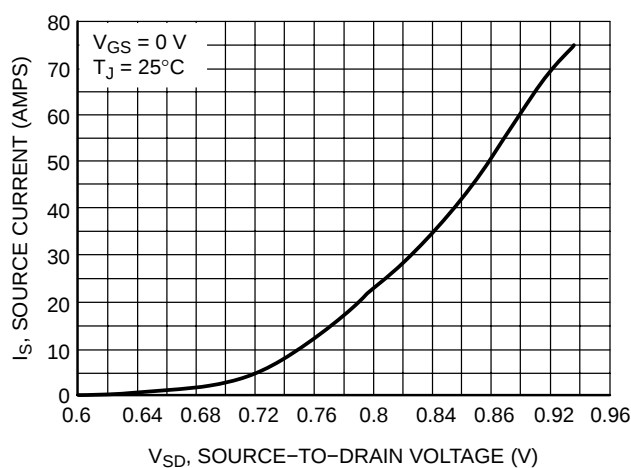


Figure 10. Diode Forward Voltage vs. Current

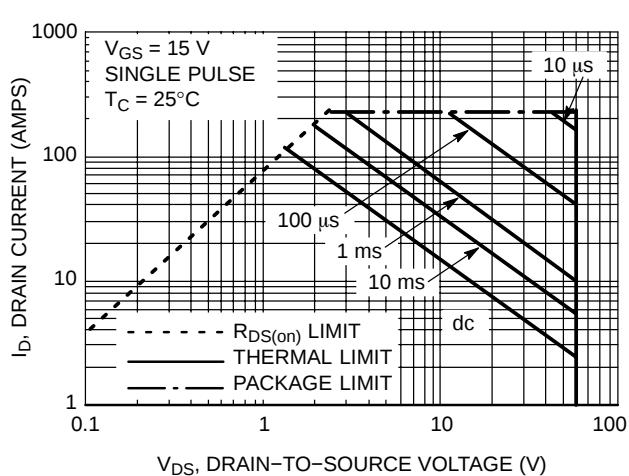


Figure 11. Maximum Rated Forward Biased Safe Operating Area

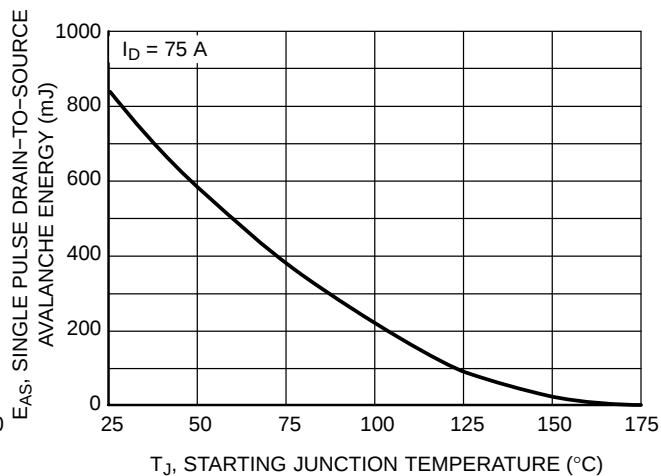


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTP75N06L, NTB75N06L

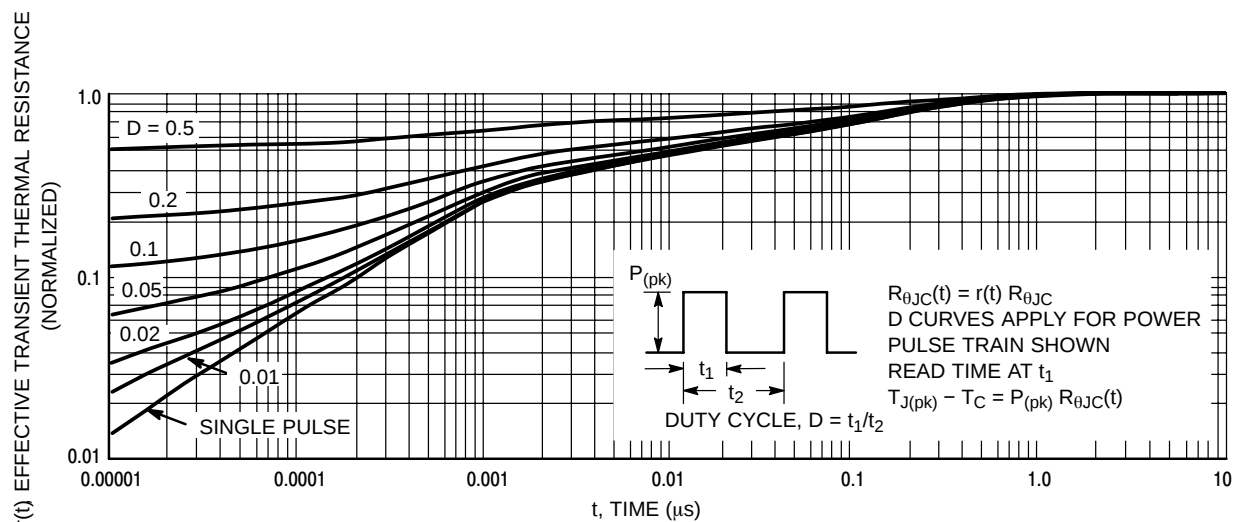


Figure 13. Thermal Response

ORDERING INFORMATION

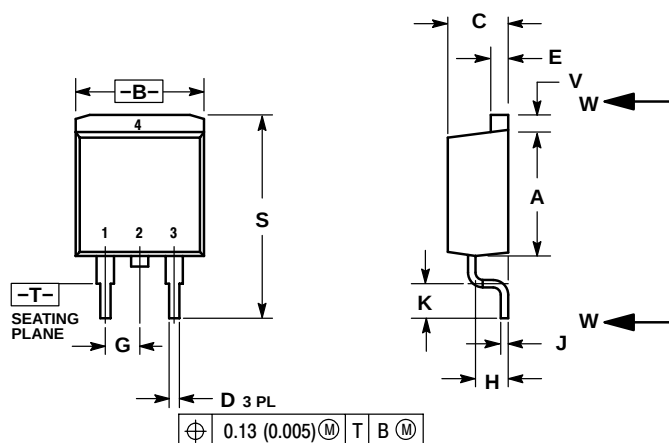
Device	Package	Shipping [†]
NTP75N06L	TO-220AB	50 Units / Rail
NTB75N06L	D ² PAK	50 Units / Rail
NTB75N06LG	D ² PAK (Pb-Free)	50 Units / Rail
NTB75N06LT4	D ² PAK	800 Units / Tape & Reel
NTB75N06LT4G	D ² PAK (Pb-Free)	800 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTP75N06L, NTB75N06L

PACKAGE DIMENSIONS

D²PAK
CASE 418B-04
ISSUE J



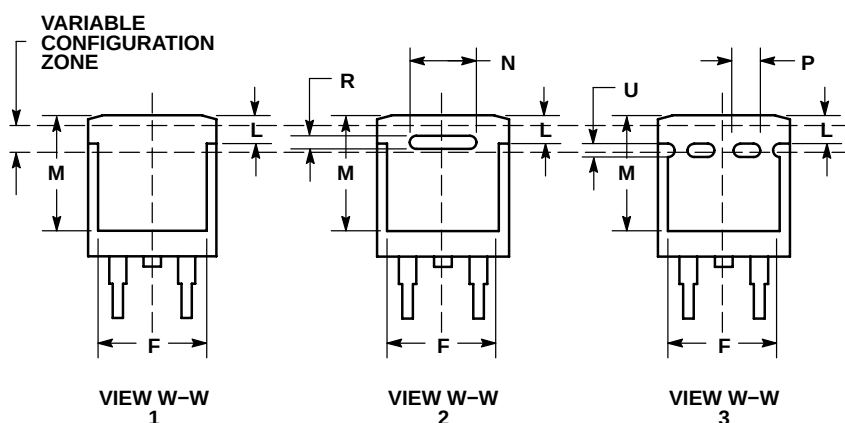
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

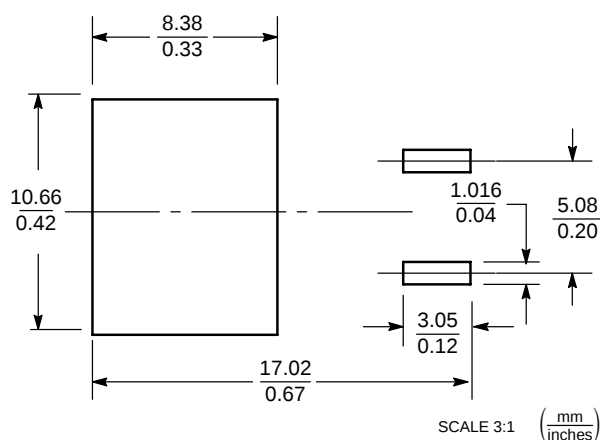
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:

- PIN 1: GATE
2: DRAIN
3: SOURCE
4: DRAIN



SOLDERING FOOTPRINT*

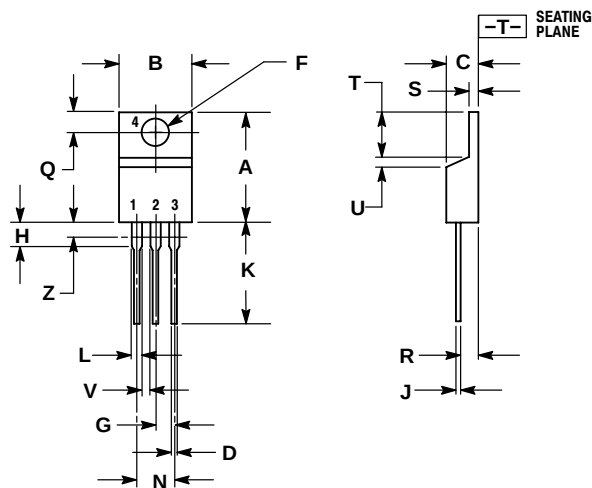


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTP75N06L, NTB75N06L

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AA



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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