Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#)
[NTQS6463R2](#)

For any questions, you can email us directly:
sales@integrated-circuit.com

NTQS6463

Power MOSFET

−20 V, −6.8 A, P−Channel TSSOP−8

Features

- New Low Profile TSSOP−8 Package
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperatures

Applications

- Power Management in Portable and Battery−Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones
- Lithium Ion Battery Applications
- Note Book PC

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−20	V
Gate−to−Source Voltage	V_{GS}	±12	V
Drain Current (Note 1) − Continuous @ T_A = 25°C − Continuous @ T_A = 70°C − Pulsed (Note 3)	 I_D I_D I_{DM}	 −5.5 −4.4 ±30	A
Total Power Dissipation (Note 1) @ T_A = 25°C	P_D	0.93	W
Drain Current (Note 2) − Continuous @ T_A = 25°C − Continuous @ T_A = 70°C − Pulsed (Note 3)	 I_D I_D I_{DM}	 −6.8 −5.4 ±30	A
Total Power Dissipation (Note 2) @ T_A = 25°C	P_D	1.39	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 40 V, I_L = 18.4 A, L = 5.0 mH, R_G = 25 Ω)	E_{AS}	845	mJ
Thermal Resistance − Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	$R_{\theta JA}$	 134 90	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

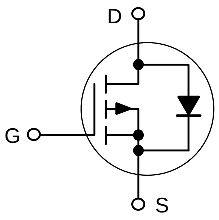
1. Minimum 3″ X 3″ FR−4 board, steady state.
2. Mounted on 1″ square (1 oz.) board, steady state.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

ON Semiconductor®

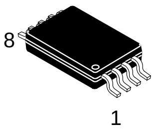
http://onsemi.com

V_{DSS}	$R_{DS(on)}$ TYP	I_D MAX
−20 V	20 mΩ @ −10 V	−6.8 A

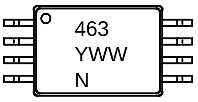
P−Channel



MARKING DIAGRAM

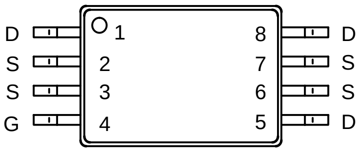


TSSOP−8
CASE 948S
PLASTIC



463 = Device Code
Y = Year
WW = Work Week
N = MOSFET

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NTQS6463	TSSOP−8	100 Units/Rail
NTQS6463R2	TSSOP−8	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2004

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
STATIC						
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = −250 μA)		$V_{GS(th)}$	−0.45	−0.9	–	V
Gate−Body Leakage (V_{GS} = 0 V, V_{GS} = ±8 V)		I_{GSS}	–	–	±100	nA
Zero Gate Threshold Voltage Drain Current		I_{DSS}				μA
(V_{DS} = −16 V, V_{GS} = 0 V)			–	–	−1.0	
(V_{DS} = −16 V, V_{GS} = 0 V, T_J = 70°C)			–	–	−10	
Drain−Source On−State Resistance (Note 4)		$R_{DS(on)}$				Ω
(V_{GS} = −4.5 V, I_D = −6.8 A)			–	0.016	0.020	
(V_{GS} = −2.5 V, I_D = −5.5 A)			–	0.022	0.027	
Forward Transconductance (V_{DS} = −15 V, I_D = −6.8 A) (Note 4)		g_{FS}	–	21	–	S
Diode Forward Voltage (I_S = −1.3 A, V_{GS} = 0 V) (Note 4)		V_{SD}	–	−0.71	−1.1	V
DYNAMIC						
Total Gate Charge	(V_{DS} = −10 V, V_{GS} = −5.0 V, I_D = −6.8 A)	Q_g	–	28	50	nC
Gate−Source Charge		Q_{gs}	–	5.5	–	
Gate−Drain Charge		Q_{gd}	–	9.0	–	
Turn−On Delay Time	(V_{DD} = −10 V, I_D ≅ −1.0 A, V_{GS} = −4.5 V, R_G = 6.0 Ω)	$t_{d(on)}$	–	15	25	ns
Rise Time		t_r	–	22	40	
Turn−Off Delay Time		$t_{d(off)}$	–	90	150	
Fall Time		t_f	–	53	90	
Source−Drain Reverse Recovery Time	(I_F = −1.3 A, di/dt = 100 A/μs)	t_{rr}	–	45	80	ns

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

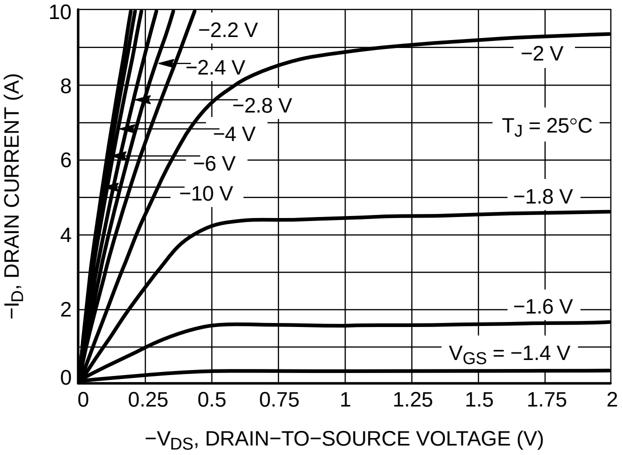


Figure 1. On−Region Characteristics

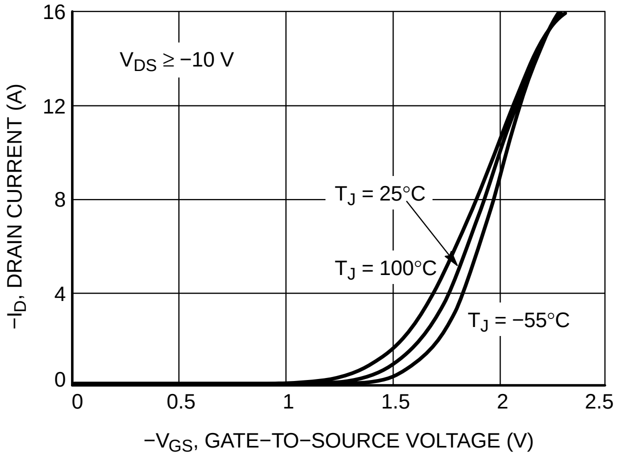


Figure 2. Transfer Characteristics

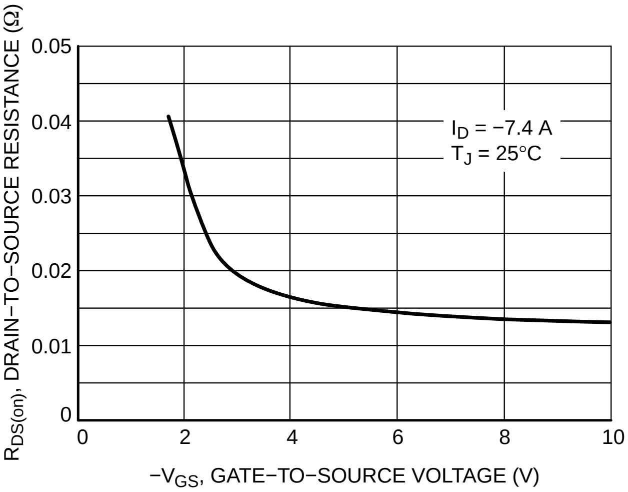


Figure 3. On−Resistance versus Gate−to−Source Voltage

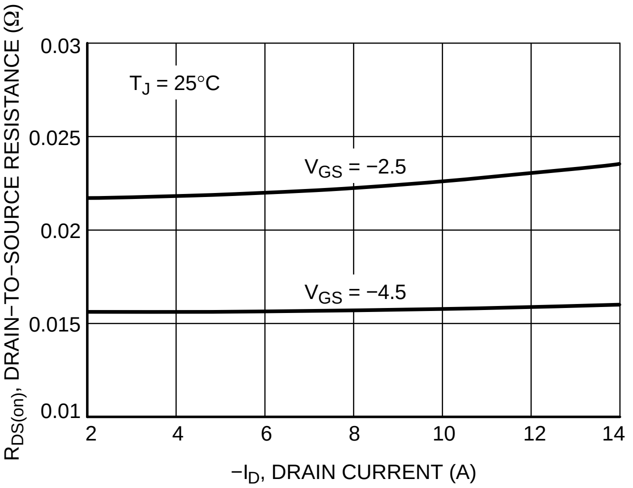


Figure 4. On−Resistance versus Drain Current and Gate Voltage

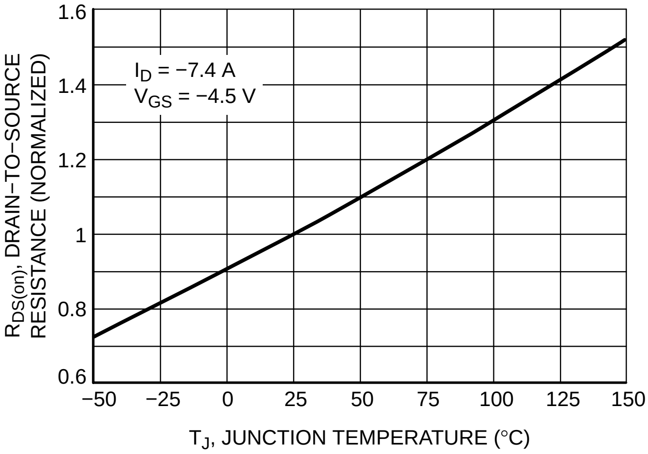


Figure 5. On−Resistance Variation versus Temperature

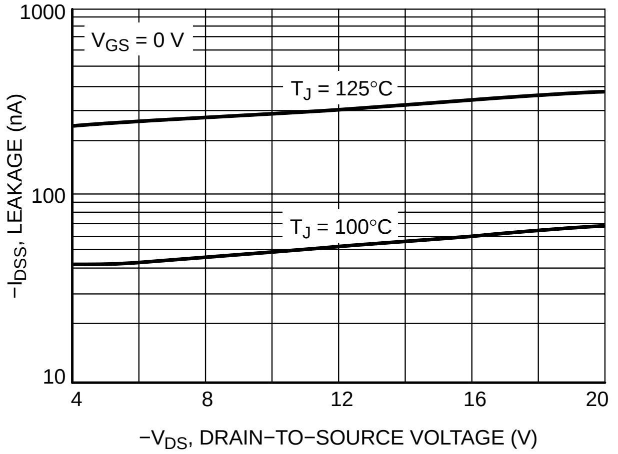


Figure 6. Drain−to−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \text{ x } R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \text{ x } R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \text{ In } [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G \, C_{iss} \text{ In } (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

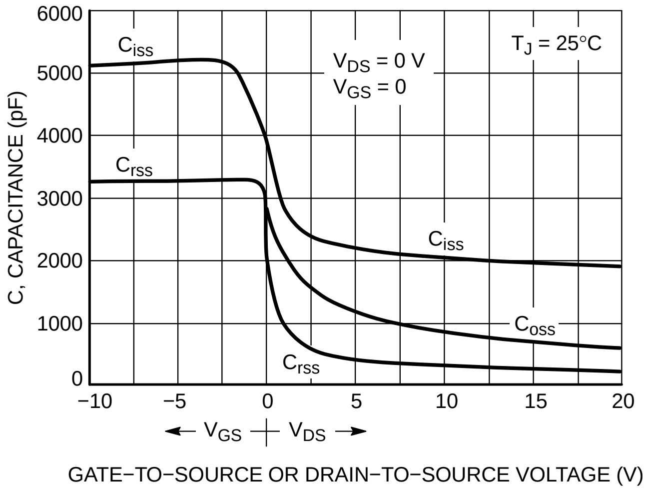


Figure 7. Capacitance Variation

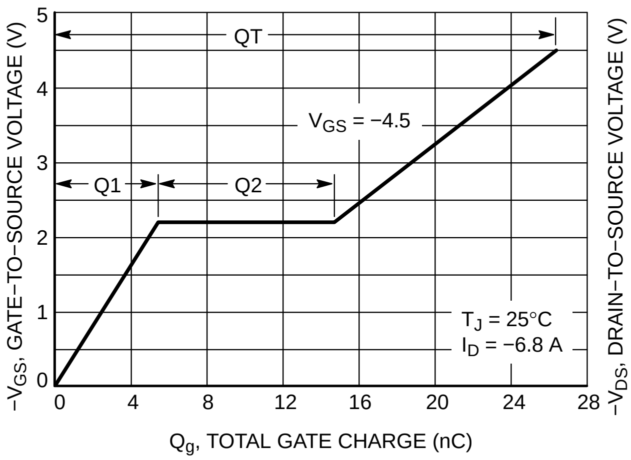


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

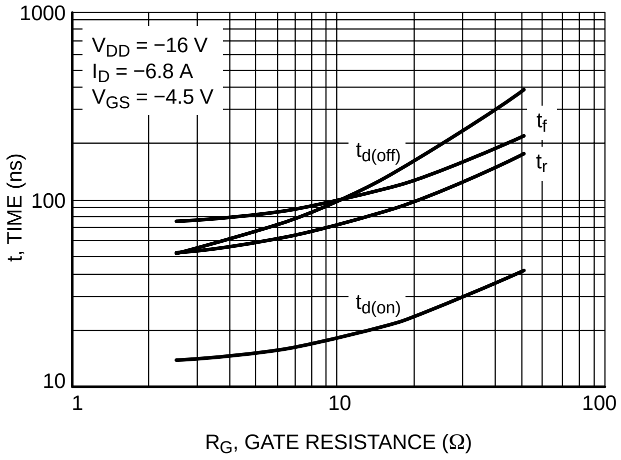


Figure 9. Resistive Switching Time Variation versus Gate Resistance

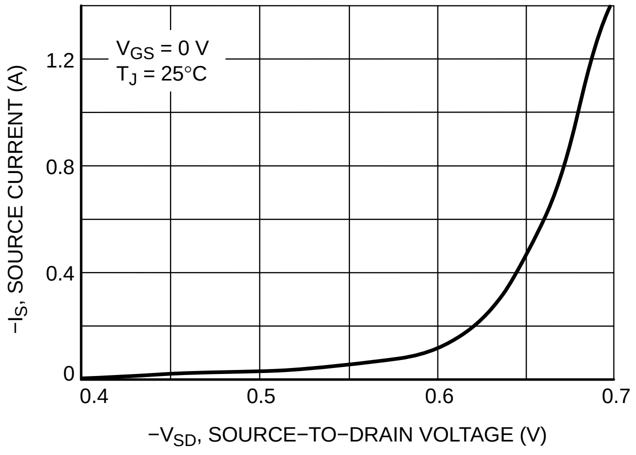


Figure 10. Diode Forward Voltage versus Current

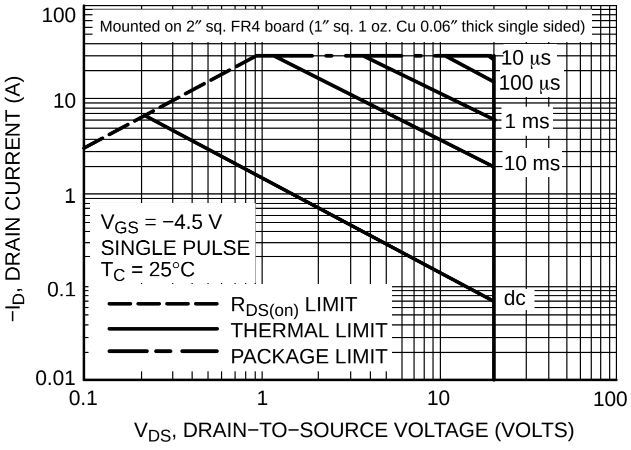


Figure 11. Maximum Rated Forward Biased Safe Operating Area

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance − General Data and Its Use.”

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r, t_f) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

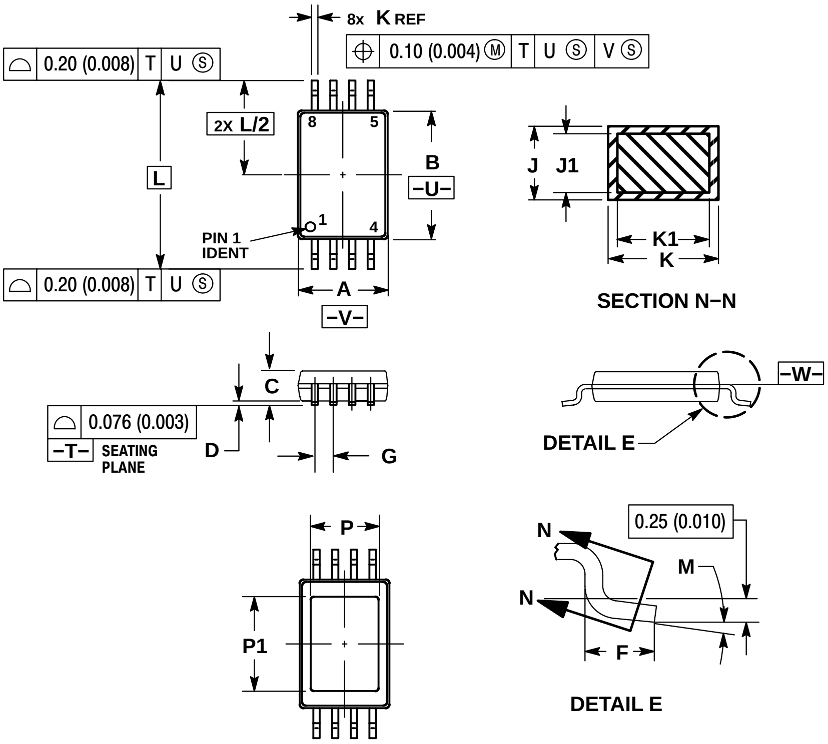
A Power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature. Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

NTQS6463

PACKAGE DIMENSIONS

TSSOP−8
CASE 948S−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°
P	---	2.20	---	0.087
P1	---	3.20	---	0.126

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.