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NZQA5V6AXV5 Series

Transient Voltage Suppressors ESD Protection Diode with Low Clamping Voltage

This integrated transient voltage suppressor device (TVS) is designed for applications requiring transient overvoltage protection. It is intended for use in sensitive equipment such as computers, printers, business machines, communication systems, medical equipment, and other applications. Its integrated design provides very effective and reliable protection for four separate lines using only one package. These devices are ideal for situations where board space is at a premium.

Features

- Low Clamping Voltage
- Small SOT-553 SMT Package
- Stand Off Voltage: 3 V
- Low Leakage Current
- Four Separate Unidirectional Configurations for Protection
- ESD Protection: IEC61000-4-2: Level 4 ESD Protection
 MILSTD 883C – Method 3015-6: Class 3
- Complies to USB 1.1 Low Speed & Full Speed Specifications
- These are Pb-Free Devices

Benefits

- Provides Protection for ESD Industry Standards: IEC 61000, HBM
- Protects Four Lines Against Transient Voltage Conditions
- Minimize Power Consumption of the System
- Minimize PCB Board Space

Typical Applications

- Instrumentation Equipment
- Serial and Parallel Ports
- Microprocessor Based Equipment
- Notebooks, Desktops, Servers
- Cellular and Portable Equipment

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

| Characteristic | Symbol | Value | Unit |
|--|---------------------------------|----------------|---------------|
| Peak Power Dissipation (Note 1) | P _{PK} | 20 | W |
| Steady State Power – 1 Diode (Note 2) | P _D | 380 | mW |
| Thermal Resistance, Junction-to-Ambient Above 25°C, Derate | R _{θJA} | 327 3.05 | °C/W mW/°C |
| Maximum Junction Temperature | T _{Jmax} | 150 | °C |
| Operating Junction and Storage Temperature Range | T _J T _{stg} | -55 to +150 | °C |
| Lead Solder Temperature (10 seconds duration) | T _L | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

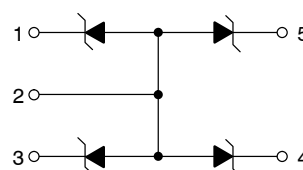
1. Non-repetitive current per Figure 5.
2. Only 1 diode under power. For all 4 diodes under power, P_D will be 25%.
 Mounted on FR-4 board with min pad.

See Application Note AND8308/D for further description of survivability specs.



ON Semiconductor®

<http://onsemi.com>



SOT-553
 CASE 463B
 PLASTIC

MARKING DIAGRAM



- xx = Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|----------|-----------------------|
| NZQA5V6AXV5T1 | SOT-553* | 4000/Tape & Reel |
| NZQA5V6AXV5T1G | SOT-553* | 4000/Tape & Reel |
| NZQA6V8AXV5T1 | SOT-553* | 4000/Tape & Reel |
| NZQA6V8AXV5T1G | SOT-553* | 4000/Tape & Reel |
| NZQA6V8AXV5T3 | SOT-553* | 16000/Tape & Reel |
| NZQA6V8AXV5T3G | SOT-553* | 16000/Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

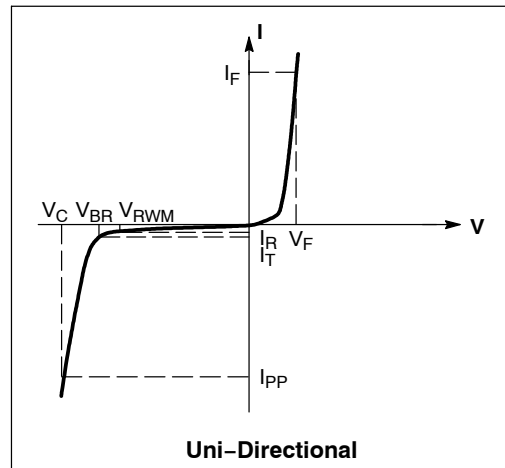
*This package is inherently Pb-Free.

NZQA5V6AXV5 Series

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

| Symbol | Parameter |
|------------------|--|
| I _{PP} | Maximum Reverse Peak Pulse Current |
| V _C | Clamping Voltage @ I _{PP} |
| V _{RWM} | Working Peak Reverse Voltage |
| I _R | Maximum Reverse Leakage Current @ V _{RWM} |
| V _{BR} | Breakdown Voltage @ I _T |
| I _T | Test Current |
| ∂V _{BR} | Maximum Temperature Coefficient of V _{BR} |
| I _F | Forward Current |
| V _F | Forward Voltage @ I _F |
| Z _{ZT} | Maximum Zener Impedance @ I _{ZT} |
| I _{ZK} | Reverse Current |
| Z _{ZK} | Maximum Zener Impedance @ I _{ZK} |



Uni-Directional

*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

| Device | Device Marking | Breakdown Voltage V _{BR} @ 1 mA (V) | | | Leakage Current I _{RM} @ V _{RM} | | V _C Max @ I _{PP} (Note 4) | | Typ Capacitance @ 0 V Bias (pF) (Note 3) | | Typ Capacitance @ 3 V Bias (pF) (Note 3) | | V _C Per IEC61000-4-2 (Note 5) |
|-------------|----------------|---|-----|------|--|----------------------|--|---------------------|---|-----|---|------|---|
| | | Min | Nom | Max | V _{RWM} | I _{RM} (μA) | V _C (V) | I _{PP} (A) | Typ | Max | Typ | Max | |
| NZQA5V6AXV5 | 5P | 5.3 | 5.6 | 5.9 | 3.0 | 1.0 | 13 | 1.6 | 13 | 17 | 7.0 | 11.5 | Figures 1 and 2 (See Below) |
| NZQA6V8AXV5 | 6H | 6.47 | 6.8 | 7.14 | 4.3 | 1.0 | 13 | 1.6 | 12 | 15 | 6.7 | 9.5 | |

3. Capacitance of one diode at f = 1 MHz, V_R = 0 V, T_A = 25°C
4. Surge current waveform per Figure 5.
5. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

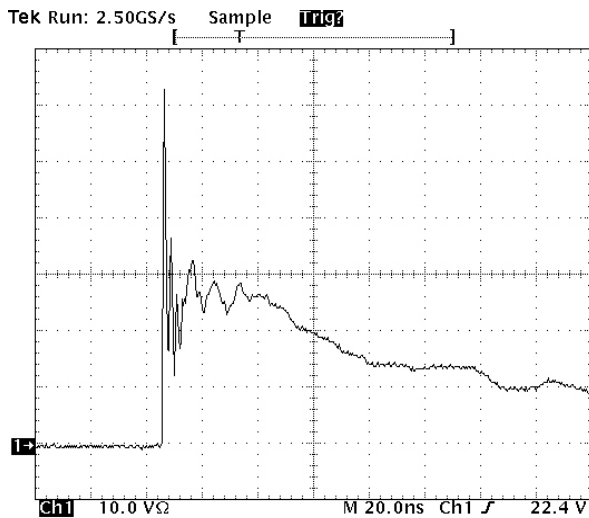


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

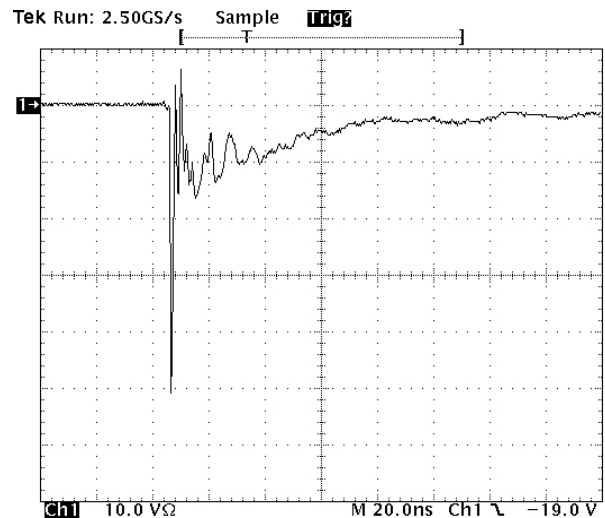


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

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IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

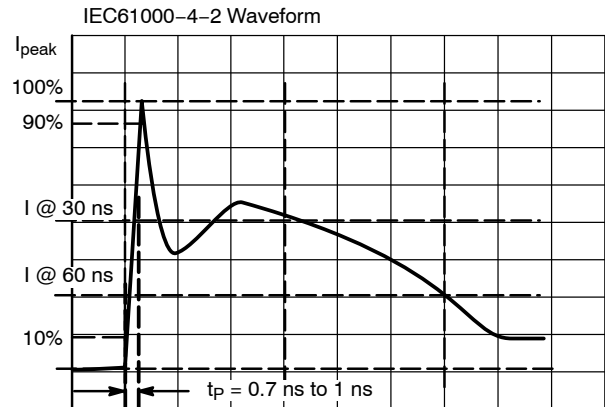


Figure 3. IEC61000-4-2 Spec

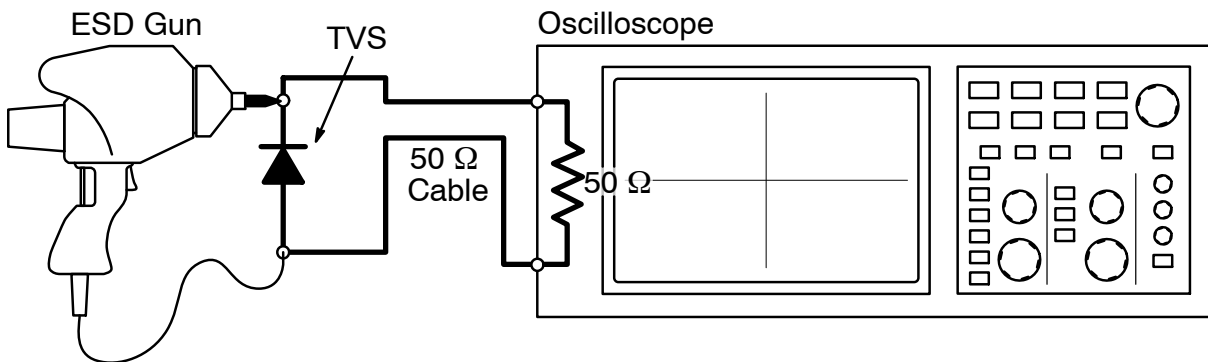


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D - Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

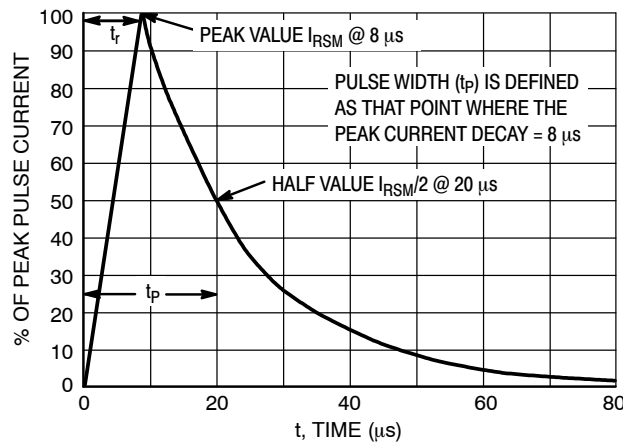


Figure 5. 8 X 20 μ s Pulse Waveform

NZQA5V6AXV5 Series

TYPICAL ELECTRICAL CHARACTERISTICS - NZQA6V8AXV5

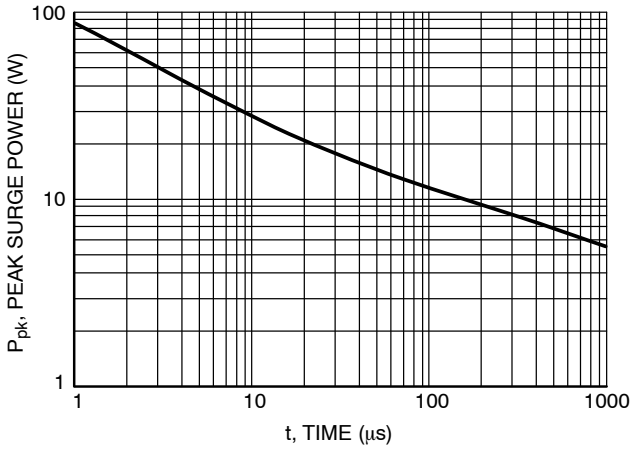


Figure 6. Pulse Width

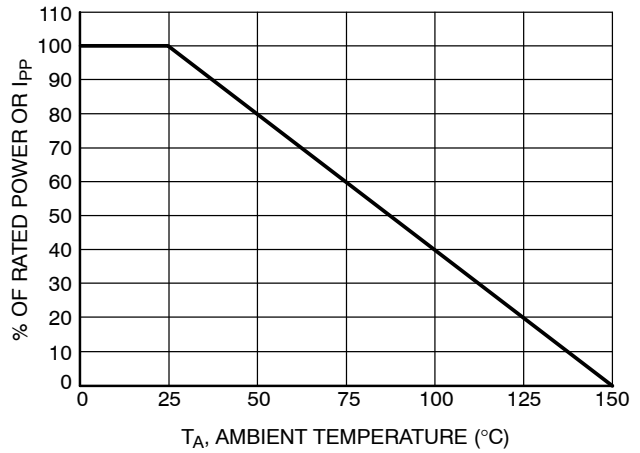


Figure 7. Power Derating Curve

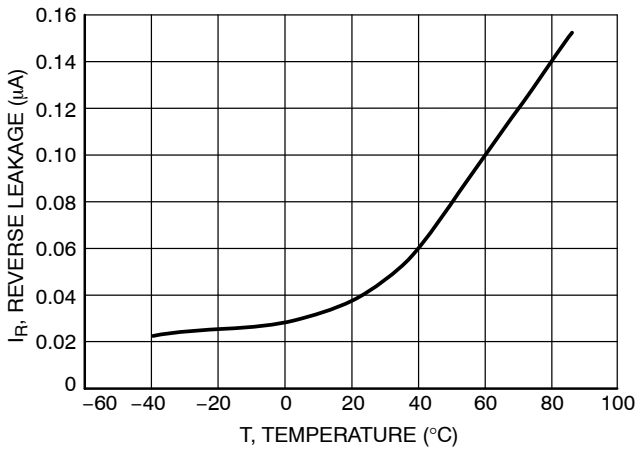


Figure 8. Reverse Leakage versus Temperature

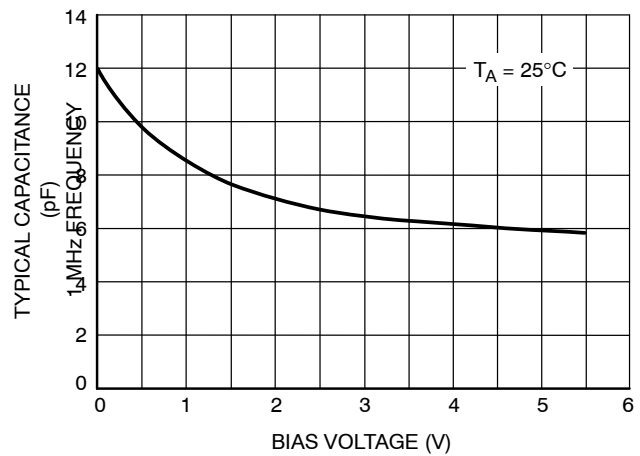


Figure 9. Capacitance

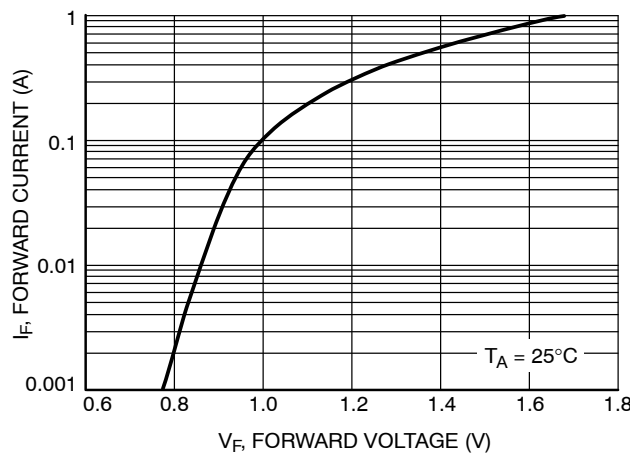
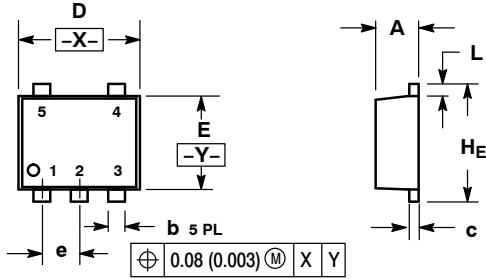


Figure 10. Forward Voltage

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PACKAGE DIMENSIONS

SOT-553, 5 LEAD
 CASE 463B-01
 ISSUE B



NOTES:

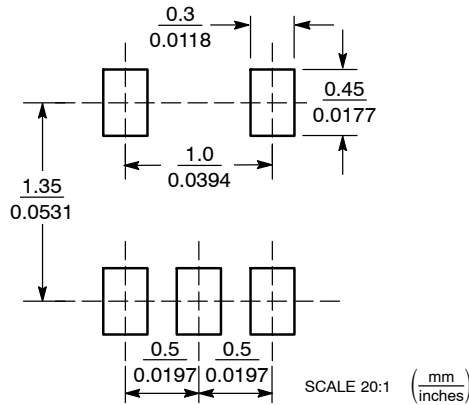
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS | | | INCHES | | |
|----------------|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| b | 0.17 | 0.22 | 0.27 | 0.007 | 0.009 | 0.011 |
| c | 0.08 | 0.13 | 0.18 | 0.003 | 0.005 | 0.007 |
| D | 1.50 | 1.60 | 1.70 | 0.059 | 0.063 | 0.067 |
| E | 1.10 | 1.20 | 1.30 | 0.043 | 0.047 | 0.051 |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| H _E | 1.50 | 1.60 | 1.70 | 0.059 | 0.063 | 0.067 |


STYLE 2:

- PIN 1. CATHODE
- COMMON ANODE
- CATHODE 2
- CATHODE 3
- CATHODE 4

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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