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# NBSG53A

## 2.5V/3.3V SiGe Selectable Differential Clock and Data D Flip-Flop/Clock Divider with Reset and OLS\*

The NBSG53A is a multi-function differential D flip-flop (DFF) or fixed divide by two (DIV/2) clock generator. This is a part of the GigaComm™ family of high performance Silicon Germanium products. A strappable control pin is provided to select between the two functions. The device is housed in a low profile 4x4 mm 16-pin Flip-Chip BGA (FCBGA) or a 3x3 mm 16 pin QFN package.

The NBSG53A is a device with data, clock, OLS, reset, and select inputs. Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The OLS input is used to program the peak-to-peak output amplitude between 0 and 800 mV in five discrete steps. The RESET and SELECT inputs are single-ended and can be driven with either LVECL or LVCMOS/LVTTL input levels.

Data is transferred to the outputs on the positive edge of the clock. The differential clock inputs of the NBSG53A allow the device to also be used as a negative edge triggered device.

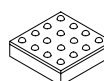
- Maximum Input Clock Frequency (DFF) > 8 GHz Typical (See Figures 4, 6, 8, 10, and 11)
  - Maximum Input Clock Frequency (DIV/2) > 10 GHz Typical (See Figures 5, 7, 9, 10, and 11)
  - 210 ps Typical Propagation Delay (OLS = FLOAT)
  - 45 ps Typical Rise and Fall Times (OLS = FLOAT)
  - DIV/2 Mode (Active with Select Low)
  - DFF Mode (Active with Select High)
  - Selectable Swing PECL Output with Operating Range:  $V_{CC} = 2.375\text{ V}$  to  $3.465\text{ V}$  with  $V_{EE} = 0\text{ V}$
  - Selectable Swing NECL Output with NECL Inputs with Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -2.375\text{ V}$  to  $-3.465\text{ V}$
  - Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak-to-Peak Output)
  - 50 Ω Internal Input Termination Resistors on all Differential Inputs
- \*Output Level Select



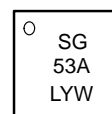
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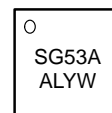
### MARKING DIAGRAM\*\*



FCBGA-16  
BA SUFFIX  
CASE 489



QFN-16  
MN SUFFIX  
CASE 485G



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*\*For further details, refer to Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
NBSG53ABA	4x4 mm FCBGA-16	100 Units/Tray
NBSG53ABAR2	4x4 mm FCBGA-16	500/Tape & Reel
NBSG53MN	3x3 mm QFN-16	123 Units/Rail
NBSG53MNR2	3x3 mm QFN-16	3000/Tape & Reel

Board	Description
NBSG53ABAEVB	NBSG53ABA Evaluation Board

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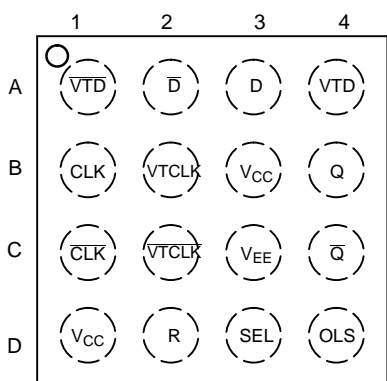


Figure 1. BGA-16 Pinout (Top View)

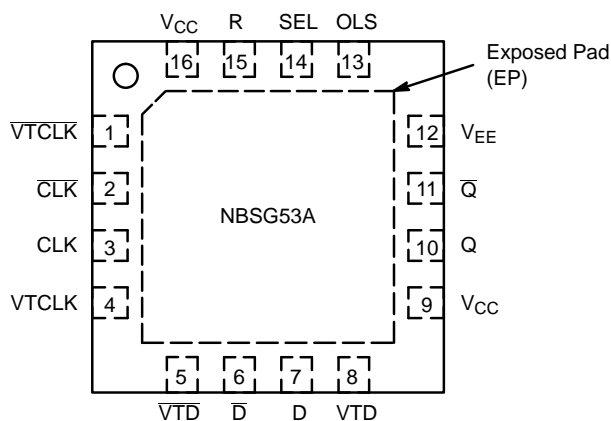


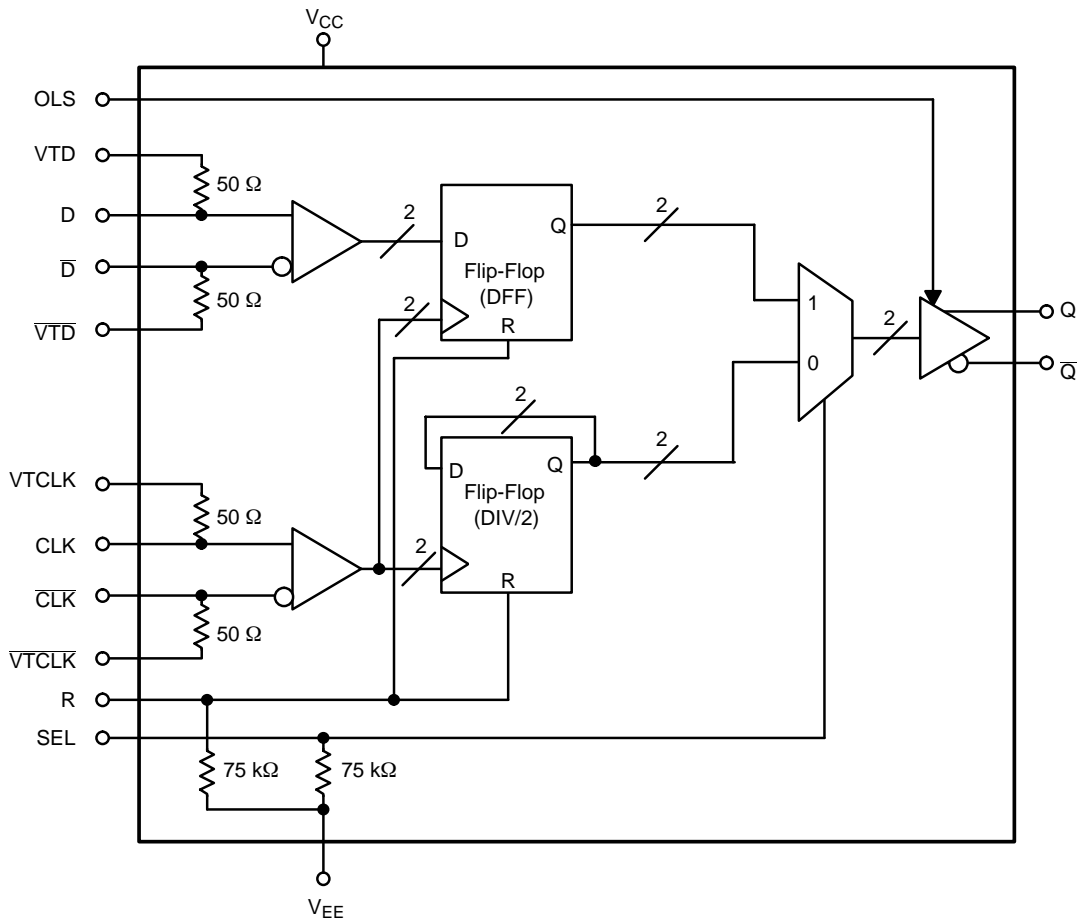
Figure 2. QFN-16 Pinout (Top View)

Table 1. Pin Description

Pin		Name	I/O	Description
BGA	QFN			
C2	1	$\overline{VTCLK}$	-	Internal 50 $\Omega$ Termination Pin. See Table 4.
C1	2	$\overline{CLK}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input.
B1	3	CLK	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input.
B2	4	VTCLK	-	Internal 50 $\Omega$ Termination Pin. See Table 4.
A1	5	$\overline{VTD}$	-	Internal 50 $\Omega$ termination pin. See Table 4.
A2	6	$\overline{D}$	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Inverted Differential Input.
A3	7	D	ECL, CML, LVCMOS, LVDS, LVTTTL Input	Noninverted Differential Input.
A4	8	VTD	-	Internal 50 $\Omega$ Termination Pin. See Table 4.
D1,B3	9,16	V <sub>CC</sub>	-	Positive Supply Voltage
B4	10	Q	RSECL Output	Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V <sub>TT</sub> = V <sub>CC</sub> - 2 V.
C4	11	$\overline{Q}$	RSECL Output	Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V <sub>TT</sub> = V <sub>CC</sub> - 2 V.
C3	12	V <sub>EE</sub>	-	Negative Supply Voltage
D4	13	OLS*	Input	Input Pin for the Output Level Select (OLS). See Table 2.
D3	14	SEL	LVECL, LVCMOS, LVTTTL Input	Select Logic Input. Internal 75 k $\Omega$ to V <sub>EE</sub> .
D2	15	R	LVECL, LVCMOS, LVTTTL Input	Reset D Flip-Flop. Internal 75 k $\Omega$ to V <sub>EE</sub> .
N/A	-	EP		Exposed Pad. (Note 1)

1. All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat-sinking conduit.
2. In the differential configuration when the input termination pins (VTD,  $\overline{VTD}$ , VTCLK,  $\overline{VTCLK}$ ) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.
3. When an output level of 400 mV is desired and V<sub>CC</sub> - V<sub>EE</sub> > 3.0 V, 2K $\Omega$  resistor should be connected from OLS pin to V<sub>EE</sub>.

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**Figure 3. Simplified Logic Diagram**

**Table 2. OUTPUT LEVEL SELECT (OLS)**

OLS	Q/Q VPP	OLS Sensitivity
V <sub>CC</sub>	800 mV	OLS - 75 mV
V <sub>CC</sub> - 0.4 V	200 mV	OLS ± 150 mV
V <sub>CC</sub> - 0.8 V	600 mV	OLS ± 100 mV
V <sub>CC</sub> - 1.2 V	0	OLS ± 75 mV
V <sub>EE</sub> (Note 4)	400 mV	OLS + 100 mV
Float	600 mV	N/A

4. When an output level of 400 mV is desired and V<sub>CC</sub> - V<sub>EE</sub> > 3.0 V, 2.0 kΩ resistor should be connected from OLS to V<sub>EE</sub>.

**Table 3. TRUTH TABLE**

R	SEL	D	CLK	Q	Function
H	x	x	x	L	Reset
L	H	L	Z	L	DFF
L	H	H	Z	H	DFF
L	L	x	Z	Q̄	DIV/2

Z = LOW to HIGH Transition

**Table 4. INTERFACING OPTIONS**

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK, VTD and VTCLK, VT̄D to V <sub>CC</sub>
LVDS	Connect VTCLK, VTD and VTCLK, VT̄D Together
AC-COUPLED	Bias VTCLK, VTD and VTCLK, VT̄D Inputs within Common Mode Range (V <sub>IHCMR</sub> )
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTTL, LVCMOS	An External Voltage (V <sub>THR</sub> ) should be Applied to the Unused Complementary Differential Input. Nominal V <sub>THR</sub> is 1.5 V for LVTTTL and V <sub>CC</sub> /2 for LVCMOS Inputs. This Voltage must be within the V <sub>THR</sub> Specification.

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**Table 5. ATTRIBUTES**

Characteristics	Value
Positive Operating Voltage Range for $V_{CC}$ ( $V_{EE} = 0$ V)	2.375 V to 3.465 V
Negative Operating Voltage Range for $V_{EE}$ ( $V_{CC} = 0$ V)	-2.375 V to -3.465 V
Internal Input Pulldown Resistor (R, SEL)	75 k $\Omega$
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 1.5 kV > 50 V > 4 kV
Moisture Sensitivity (Note 5)	16-FCBGA 16-QFN
	Level 3 Level 1
Flammability Rating	UL 94 V-0 @ 0.125 in
Oxygen Index	28 to 34
Transistor Count	482
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

5. For additional information, refer to Application Note AND8003/D.

**Table 6. MAXIMUM RATINGS** (Note 6)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
$V_{CC}$	Positive Power Supply	$V_{EE} = 0$ V		3.6	V
$V_{EE}$	Negative Power Supply	$V_{CC} = 0$ V		-3.6	V
$V_I$	Positive Input Negative Input	$V_{EE} = 0$ V $V_{CC} = 0$ V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 -3.6	V V
$V_{INPP}$	Differential Input Voltage  D - $\bar{D}$	$V_{CC} - V_{EE} \geq 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8   $V_{CC} - V_{EE}$	V V
$I_{IN}$	Input Current Through $R_T$ (50 $\Omega$ Resistor)	Static Surge		45 80	mA mA
$I_{OUT}$	Output Current	Continuous Surge		25 50	mA mA
$T_A$	Operating Temperature Range	16 FCBGA 16 QFN		-40 to +70 -40 to +85	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}$ C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 7)	0 LFPM 500 LFPM 0 LFPM 500 LFPM	16 FCBGA 16 FCBGA 16 QFN 16 QFN	108 86 41.6 35.2	$^{\circ}$ C/W $^{\circ}$ C/W $^{\circ}$ C/W $^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	2S2P (Note 7) 2S2P (Note 8)	16 FCBGA 16 QFN	5.0 4.0	$^{\circ}$ C/W $^{\circ}$ C/W
$T_{sol}$	Wave Solder	< 15 Seconds		225	$^{\circ}$ C

6. Maximum Ratings are those values beyond which device damage may occur.

7. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power).

8. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 7. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT**  $V_{CC} = 2.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 9)

Symbol	Characteristic	-40 °C			25 °C			70 °C(BGA)/85 °C(QFN)**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current	33	45	57	33	45	57	33	45	57	mA
$V_{OH}$	Output HIGH Voltage (Note 10)	1460	1510	1560	1490	1540	1590	1515	1565	1615	mV
$V_{OL}$	Output LOW Voltage (Note 10)										mV
	(OLS = $V_{CC}$ )	555	705	855	595	745	895	625	775	925	
	(OLS = $V_{CC} - 0.4\text{ V}$ )	1235	1295	1355	1270	1330	1390	1295	1355	1415	
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	775	895	1015	810	930	1050	840	960	1080	
	(OLS = $V_{CC} - 1.2\text{ V}$ )	1455	1505	1555	1490	1540	1590	1510	1560	1610	
	(OLS = $V_{EE}$ )	1005	1095	1185	1040	1130	1220	1065	1155	1245	
$V_{OUTPP}$	Output Voltage Amplitude										mV
	(OLS = $V_{CC}$ )	715	805		705	795		700	790		
	(OLS = $V_{CC} - 0.4\text{ V}$ )	125	215		120	210		120	210		
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	525	615		520	610		515	605		
	(OLS = $V_{CC} - 1.2\text{ V}$ )	0	5		0	0		0	5		
	(OLS = $V_{EE}$ )	325	415		320	410		320	410		
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Notes 12 and 14) CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) (Notes 13 and 14) CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$	$V_{EE}$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{EE}$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{EE}$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
$V_{IH}$	Input High Voltage (Single-Ended) R, SEL	1290		$V_{CC}$	1355		$V_{CC}$	1415		$V_{CC}$	mV
$V_{IL}$	Input Low Voltage (Single-Ended) R, SEL	$V_{EE}$		890	$V_{EE}$		955	$V_{EE}$		1015	mV
$V_{THR}$	Input Threshold Voltage (Single-Ended) (Note 14)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 11)	1.2		2.5	1.2		2.5	1.2		2.5	V
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ ) R, SEL CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$		35 5	100 50		35 5	100 50		35 5	100 50	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) R, SEL CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$		20 5	100 50		20 5	100 50		20 5	100 50	$\mu\text{A}$

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.125 V to -0.965 V.

10. All outputs loaded with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

11.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

12.  $V_{IH}$  cannot exceed  $V_{CC}$ .  $|V_{IH} - V_{THR}| < 2600\text{ mV}$ .

13.  $V_{IL}$  always  $\geq V_{EE}$ .  $|V_{IL} - V_{THR}| < 2600\text{ mV}$ .

14.  $V_{THR}$  is the voltage applied to one input when running in single-ended mode.

\*Typicals used for testing purposes.

\*\*The device packaged in FCBGA-16 have maximum ambient temperature specification of 70 °C and devices packaged in QFN-16 have maximum ambient temperature specification of 85 °C.

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**Table 8. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 15)

Symbol	Characteristic	-40 °C			25 °C			70 °C(BGA)/85 °C(QFN)***			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current	35	47	59	35	47	59	35	47	59	mA
$V_{OH}$	Output HIGH Voltage (Note 16)	2260	2310	2360	2290	2340	2390	2315	2365	2415	mV
$V_{OL}$	Output LOW Voltage (Note 16)										mV
	(OLS = $V_{CC}$ )	1320	1470	1620	1360	1510	1660	1390	1540	1690	
	(OLS = $V_{CC} - 0.4\text{ V}$ )	2030	2090	2150	2065	2125	2185	2090	2150	2210	
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	1550	1670	1790	1585	1705	1825	1615	1735	1855	
	(OLS = $V_{CC} - 1.2\text{ V}$ )	2260	2310	2360	2290	2340	2390	2315	2365	2415	
	** (OLS = $V_{EE}$ )	1785	1875	1965	1820	1910	2000	1850	1940	2030	
$V_{OUTPP}$	Output Amplitude Voltage										mV
	(OLS = $V_{CC}$ )	750	840		740	830		735	825		
	(OLS = $V_{CC} - 0.4\text{ V}$ )	130	220		125	215		125	215		
	(OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT)	550	640		545	635		540	630		
	(OLS = $V_{CC} - 1.2\text{ V}$ )	0	0		0	0		0	0		
	** (OLS = $V_{EE}$ )	345	435		340	430		335	425		
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Notes 18 and 20) CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) (Notes 19 and 20) CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
$V_{IH}$	Input High Voltage (Single-Ended) R, SEL	2090		$V_{CC}$	2155		$V_{CC}$	2215		$V_{CC}$	mV
$V_{IL}$	Input Low Voltage (Single-Ended) R, SEL	$V_{EE}$		1690	$V_{EE}$		1755	$V_{EE}$		1815	mV
$V_{THR}$	Input Threshold Voltage (Single-Ended) (Note 20)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 17)	1.2		3.3	1.2		3.3	1.2		3.3	V
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ ) R, SEL CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$		35 5	100 50		35 5	100 50		35 5	100 50	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) R, SEL CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$		20 5	100 50		20 5	100 50		20 5	100 50	$\mu\text{A}$

NOTE: GigaComm Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

15. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925 V to -0.165 V.

16. All outputs loaded with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

17.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

18.  $V_{IH}$  cannot exceed  $V_{CC}$ .  $|V_{IH} - V_{THR}| < 2600\text{ mV}$ .

19.  $V_{IL}$  always  $\geq V_{EE}$ .  $|V_{IL} - V_{THR}| < 2600\text{ mV}$ .

20.  $V_{THR}$  is the voltage applied to one input when running in single-ended mode.

\*Typicals used for testing purposes.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

\*\*\*The device packaged in FCBGA-16 have maximum ambient temperature specification of 70 °C and devices packaged in QFN-16 have maximum ambient temperature specification of 85 °C.

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**Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT**

$V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  (Note 21)

Symbol	Characteristic	-40 °C			25 °C			70 °C(BGA)/85 °C(QFN)***			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Negative Power Supply Current	35	47	59	35	47	59	35	47	59	mA
$V_{OH}$	Output HIGH Voltage (Note 22)	-1040	-990	-940	-1010	-960	-910	-985	-935	-885	mV
$V_{OL}$	Output LOW Voltage (Note 22) $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ (OLS = $V_{CC}$ ) (OLS = $V_{CC} - 0.4\text{ V}$ ) (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$ ) ** (OLS = $V_{EE}$ ) $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$ (OLS = $V_{CC}$ ) (OLS = $V_{CC} - 0.4\text{ V}$ ) (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$ ) (OLS = $V_{EE}$ )	-1980 -1270 -1750 -1040 -1515 -1945 -1265 -1725 -1045 -1495	-1830 -1210 -1630 -990 -1425 -1795 -1205 -1605 -995 -1405	-1680 -1150 -1510 -940 -1335 -1645 -1145 -1485 -945 -1315	-1940 -1235 -1715 -1010 -1480 -1905 -1230 -1690 -1010 -1460	-1790 -1175 -1595 -960 -1390 -1755 -1170 -1570 -960 -1370	-1640 -1115 -1475 -910 -1300 -1605 -1110 -1450 -910 -1280	-1910 -1210 -1685 -985 -1450 -1875 -1205 -1660 -990 -1435	-1760 -1150 -1565 -935 -1360 -1725 -1145 -1540 -940 -1345	-1610 -1090 -1445 -885 -1270 -1575 -1085 -1420 -890 -1255	mV
$V_{OUTPP}$	Output Voltage Amplitude $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ (OLS = $V_{CC}$ ) (OLS = $V_{CC} - 0.4\text{ V}$ ) (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$ ) ** (OLS = $V_{EE}$ ) $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$ (OLS = $V_{CC}$ ) (OLS = $V_{CC} - 0.4\text{ V}$ ) (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$ ) (OLS = $V_{EE}$ )	750 130 550 0 345 715 125 525 0 325	840 220 640 0 435 805 215 615 5 415		740 125 545 0 340 705 120 520 0 320	830 215 635 0 430 795 210 610 0 410		735 125 540 0 335 700 120 515 0 320	825 215 630 0 425 790 210 605 5 410		mV
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Notes 24 and 26) CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	$V_{EE} + 1275$	$V_{CC} - 1000^*$	$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) (Notes 25 and 26) CLK, $\overline{\text{CLK}}$ , D, $\overline{\text{D}}$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	$V_{IH} - 2600$	$V_{CC} - 1400^*$	$V_{IH} - 150$	mV
$V_{IH}$	Input High Voltage (Single-Ended) R, SEL	-1210		$V_{CC}$	-1145		$V_{CC}$	-1085		$V_{CC}$	mV
$V_{IL}$	Input Low Voltage (Single-Ended) R, SEL	$V_{EE}$		-1610	$V_{EE}$		-1545	$V_{EE}$		-1485	mV
$V_{THR}$	Input Threshold Voltage (Single-Ended) (Note 26)	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	$V_{EE} + 1125$		$V_{CC} - 75$	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 23)	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	$V_{EE} + 1.2$		0.0	V

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

21. Input and output parameters vary 1:1 with  $V_{CC}$ .

22. All outputs loaded with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

23.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

24.  $V_{IH}$  cannot exceed  $V_{CC}$ .  $|V_{IH} - V_{THR}| < 2600\text{ mV}$ .

25.  $V_{IL}$  always  $\geq V_{EE}$ .  $|V_{IL} - V_{THR}| < 2600\text{ mV}$ .

26.  $V_{THR}$  is the voltage applied to one input when running in single-ended mode.

\*Typicals used for testing purposes.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

\*\*\*The device packaged in FCBGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.



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**Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT**

$V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V}$  to  $-2.375\text{ V}$  (Note 21) (continued)

Symbol	Characteristic	-40 °C			25 °C			70 °C(BGA)/85 °C(QFN)***			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$R_{TIN}$	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	$\Omega$
$I_{IH}$	Input HIGH Current (@ $V_{IH}$ ) R, SEL CLK, $\overline{CLK}$ , D, $\overline{D}$		35 5	100 50		35 5	100 50		35 5	100 50	$\mu\text{A}$
$I_{IL}$	Input LOW Current (@ $V_{IL}$ ) R, SEL CLK, $\overline{CLK}$ , D, $\overline{D}$		20 5	100 50		20 5	100 50		20 5	100 50	$\mu\text{A}$
$I_{OLS}$	OLS Input Current (See Figure 12) (OLS = $V_{CC}$ ) (OLS = $V_{CC} - 0.4\text{ V}$ ) (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$ ) $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ *(OLS = $V_{EE}$ ) $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$ (OLS = $V_{EE}$ )		300 100 5 -1500 -1000	900 300 100 -600 -400		300 100 5 -1500 -1000	900 300 100 -600 -400		300 100 5 -600 -400	900 300 100 -600 -400	$\mu\text{A}$

NOTE: GigaComm circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

21. Input and output parameters vary 1:1 with  $V_{CC}$ .

22. All outputs loaded with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

23.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

24.  $V_{IH}$  cannot exceed  $V_{CC}$ .  $|V_{IH} - V_{THR}| < 2600\text{ mV}$ .

25.  $V_{IL}$  always  $\geq V_{EE}$ .  $|V_{IL} - V_{THR}| < 2600\text{ mV}$ .

26.  $V_{THR}$  is the voltage applied to one input when running in single-ended mode.

\*Typicals used for testing purposes.

\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

\*\*\*The device packaged in FCBGA-16 have maximum ambient temperature specification of 70 °C and devices packaged in QFN-16 have maximum ambient temperature specification of 85 °C.

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**Table 10. AC CHARACTERISTICS for FCBGA-16**

$V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V to } -2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V to } 3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40 °C			25 °C			70 °C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f <sub>max</sub>	Maximum Frequency (See Figures 4, 6, 8, 10, and 11) DFF		8			8			8		GHz	
	(See Figures 5, 7, 9, 10, and 11) DIV/2		10			10			10			
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay to Output Differential CLK→Q, $\bar{Q}$ (OLS = V <sub>CC</sub> )		160	210	260	160	215	270	165	220	275	ps
		(OLS = V <sub>CC</sub> - 0.4 V)	150	200	250	155	205	255	160	210	260	
		(OLS = V <sub>CC</sub> - 0.8 V, OLS = FLOAT)	155	205	255	160	210	260	160	215	270	
		** (OLS = V <sub>EE</sub> )	155	205	255	160	210	260	160	215	270	
	SEL→Q, $\bar{Q}$ (OLS = V <sub>CC</sub> )		165	220	275	170	225	280	170	225	280	
		(OLS = V <sub>CC</sub> - 0.4 V)	160	210	260	160	210	260	160	210	260	
		(OLS = V <sub>CC</sub> - 0.8 V, OLS = FLOAT)	160	215	270	165	220	275	165	220	275	
		** (OLS = V <sub>EE</sub> )	160	210	260	160	215	270	165	220	275	
	R→Q, $\bar{Q}$ (OLS = V <sub>CC</sub> ) DIV/2		220	295	370	225	300	375	225	300	375	
		(OLS = V <sub>CC</sub> ) DFF	200	270	340	205	275	345	205	275	345	
		(OLS = V <sub>CC</sub> - 0.4 V) DIV/2	215	285	355	220	290	360	220	290	360	
		(OLS = V <sub>CC</sub> - 0.4 V) DFF	195	260	325	200	265	330	200	265	330	
(OLS = V <sub>CC</sub> - 0.8 V, OLS = FLOAT) DIV/2		220	290	360	220	295	370	220	295	370		
(OLS = V <sub>CC</sub> - 0.8 V, OLS = FLOAT) DFF		200	265	330	200	270	340	200	270	340		
** (OLS = V <sub>EE</sub> ) DIV/2		215	285	355	220	290	360	220	290	360		
** (OLS = V <sub>EE</sub> ) DFF		195	260	325	200	265	330	200	265	330		
t <sub>SKEW</sub>	Duty Cycle Skew (Notes 28 and 30) DFF		5	20		5	20		5	20	ps	
t <sub>JITTER</sub>	RMS Random Clock Jitter f <sub>in</sub> ≤ 8 GHz		0.5	1.5		0.5	1.5		0.5	1.5	ps	
	(See Figures 4 and 6) (Note 27) Peak-to-Peak Data Dependent Jitter f <sub>in</sub> = 8 Gb/s					TBD						
V <sub>INPP</sub>	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 29)	75		2600	75		2600	75		2600	mV	
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times (20% - 80%) @ 1 GHz Q, $\bar{Q}$ (OLS = V <sub>CC</sub> )		30	50	65	30	50	65	30	50	65	ps
		(OLS = V <sub>CC</sub> - 0.4 V)	20	40	60	20	40	60	20	40	60	
		(OLS = V <sub>CC</sub> - 0.8 V, OLS = FLOAT)	25	45	65	25	45	65	25	45	65	
		** (OLS = V <sub>EE</sub> )	25	45	65	25	45	65	25	45	65	
t <sub>s</sub>	Setup Time D→CLK	30	14		30	10		30	13		ps	
t <sub>h</sub>	Hold Time D→CLK	25	12		25	7		25	9		ps	
t <sub>rr</sub>	Reset Recovery DFF, DIV/2	40	9		40	12		40	10		ps	

27. Measured using a 500 mV source, 50% duty cycle clock source. Repetitive 1010 input data pattern. All outputs loaded with 50 Ω to

V<sub>CC</sub> - 2.0 V. Input edge rates is 40 ps (20% - 80%).

28. See Figure 14. t<sub>SKEW</sub> = |t<sub>PLH</sub> - t<sub>PHL</sub>| for a nominal 50% differential clock input waveform.

29. V<sub>INPP</sub> (MAX) cannot exceed V<sub>CC</sub> - V<sub>EE</sub> (Applicable only when V<sub>CC</sub> - V<sub>EE</sub> < 2600 mV).

30. See Figure 10. Duty Cycle % vs. Frequency.

\*\*When an output level of 400 mV is desired and V<sub>CC</sub> - V<sub>EE</sub> > 3.0 V, a 2 kΩ resistor should be connected from OLS to V<sub>EE</sub>.

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**Table 11. AC CHARACTERISTICS for QFN-16**

$V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.465\text{ V to }-2.375\text{ V}$  or  $V_{CC} = 2.375\text{ V to }3.465\text{ V}$ ;  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$f_{max}$	Maximum Frequency (See Figures 4, 6, 8, 10, and 11) DFF (See Figures 5, 7, 9, 10, and 11) DIV/2 (Note 31)		8			8			8		GHz	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential (Note 35) CLK→Q, $\bar{Q}$ SEL→Q, $\bar{Q}$ R→Q, $\bar{Q}$ $D_{IN}/2$ DFF	150 160 215 195	215 190 280 270	285 280 375 345	150 160 215 195	215 190 280 270	285 280 375 345	150 160 215 195	215 190 280 270	285 280 375 345	ps	
$t_{SKEW}$	Duty Cycle Skew (Notes 32 and 34) DFF		5	20		5	20		5	20	ps	
$t_{JITTER}$	RMS Random Clock Jitter $f_{in} \leq 8\text{ GHz}$ (See Figures 4 and 6) (Note 31) Peak-to-Peak Data Dependent Jitter $f_{in} = 8\text{ Gb/s}$		0.5	1		0.5	1		0.5	1	ps	
$V_{INPP}$	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 33)	75		2600	75		2600	75		2600	mV	
$t_r$ $t_f$	Output Rise/Fall Times (20% - 80%) @ 1 GHz Q, $\bar{Q}$ (OLS = $V_{CC}$ ) (OLS = $V_{CC} - 0.4\text{ V}$ ) (OLS = $V_{CC} - 0.8\text{ V}$ , OLS = FLOAT) **(OLS = $V_{EE}$ )		28 15 25 20	40 40 35 35	65 65 65 65	28 15 25 20	40 40 35 35	65 65 65 65	28 15 25 20	40 40 35 35	65 65 65 65	ps
$t_s$	Setup Time D→CLK	30	14		30	10		30	13		ps	
$t_h$	Hold Time D→CLK	25	12		25	7		25	0		ps	
$t_{rr}$	Reset Recovery DFF, DIV/2	40	9		40	12		40	10		ps	

31. Measured using a 500 mV source, 50% duty cycle clock source. Repetitive 1010 input data pattern. All outputs loaded with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ . Input edge rates is 40 ps (20% - 80%).

32. See Figure 14.  $t_{SKEW} = |t_{PLH} - t_{PHL}|$  for a nominal 50% differential clock input waveform.

33.  $V_{INPP}$  (MAX) cannot exceed  $V_{CC} - V_{EE}$  (Applicable only when  $V_{CC} - V_{EE} < 2600\text{ mV}$ ).

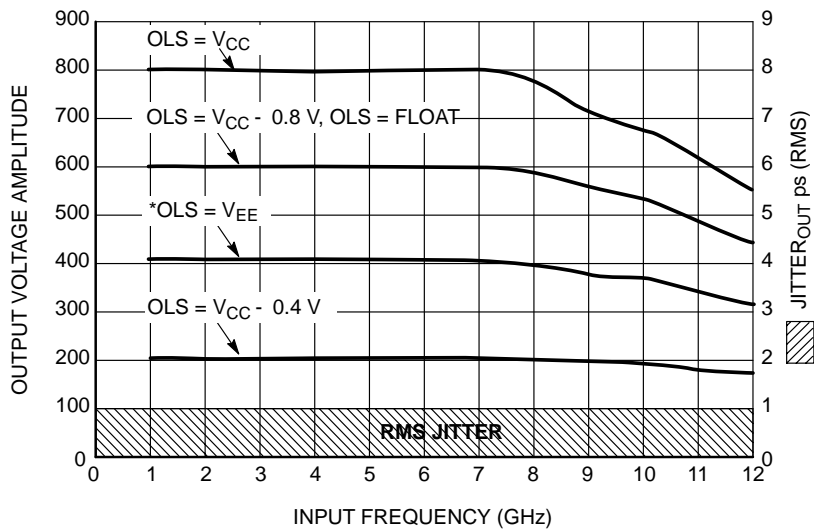
34. See Figure 10. Duty Cycle % vs. Frequency.

35. For all OLS Configuration.

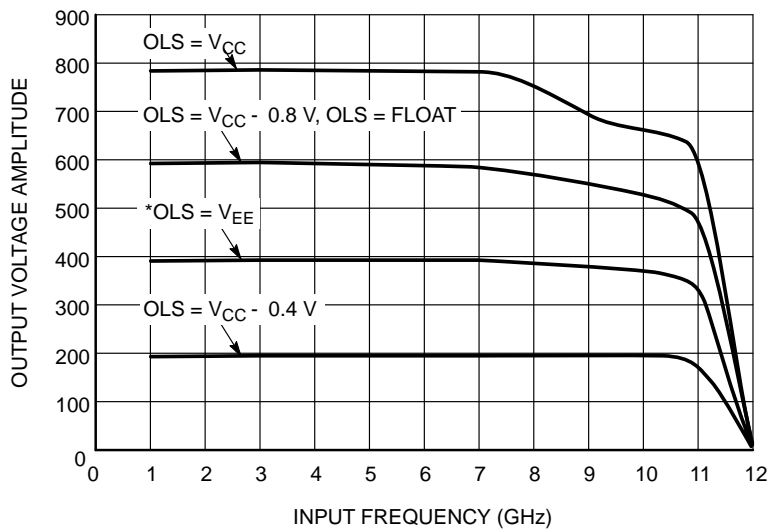
\*\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a 2 k $\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

\*\*\*The device packaged in FCBGA-16 have maximum ambient temperature specification of 70°C and devices packaged in QFN-16 have maximum ambient temperature specification of 85°C.

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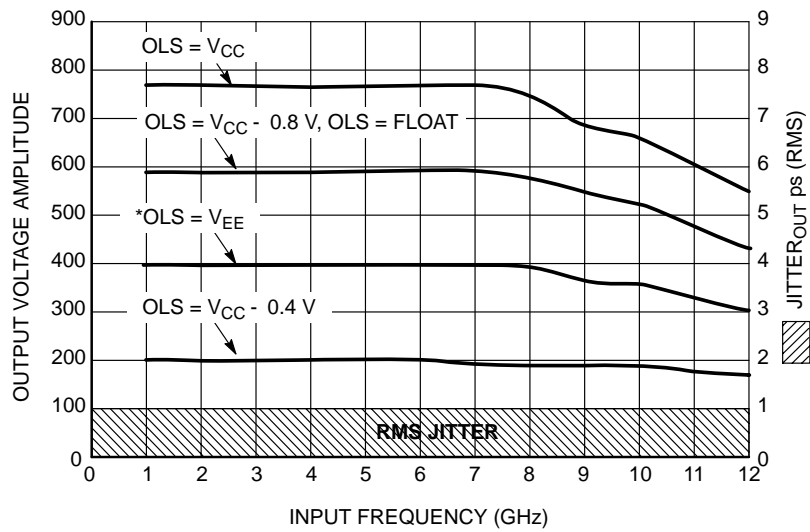
**Figure 4. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for DFF Mode ( $V_{CC} - V_{EE} = 3.3\text{ V}$  @  $25^\circ\text{C}$ ; Repetitive 1010 Input Data Pattern)**



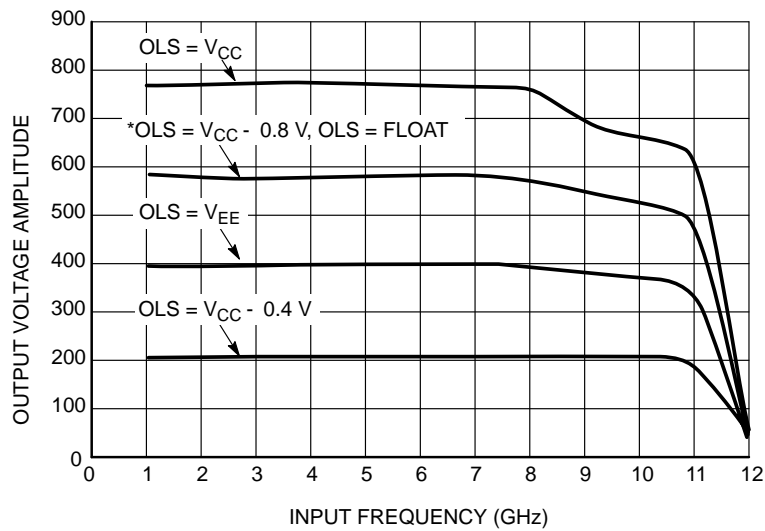
**Figure 5. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for DIV/2 Mode ( $V_{CC} - V_{EE} = 3.3\text{ V}$  @  $25^\circ\text{C}$ )**

\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a  $2\text{ k}\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

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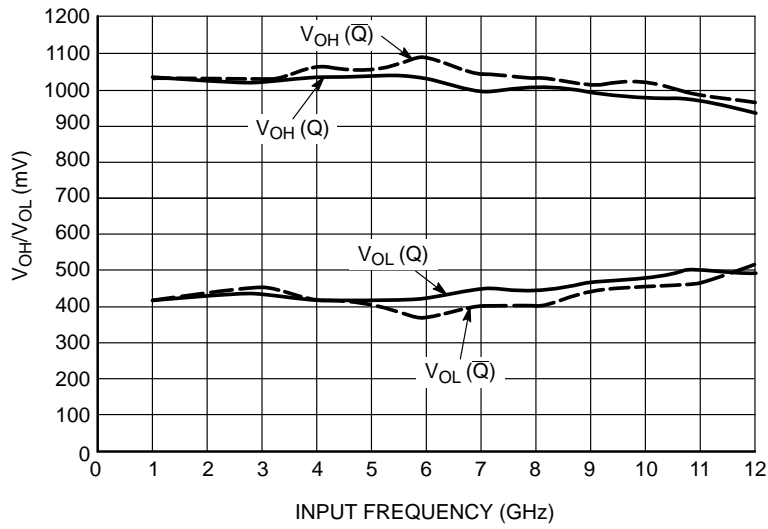
**Figure 6. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for DFF Mode ( $V_{CC} - V_{EE} = 2.5\text{ V}$  @  $25^\circ\text{C}$ ; Repetitive 1010 Input Data Pattern)**



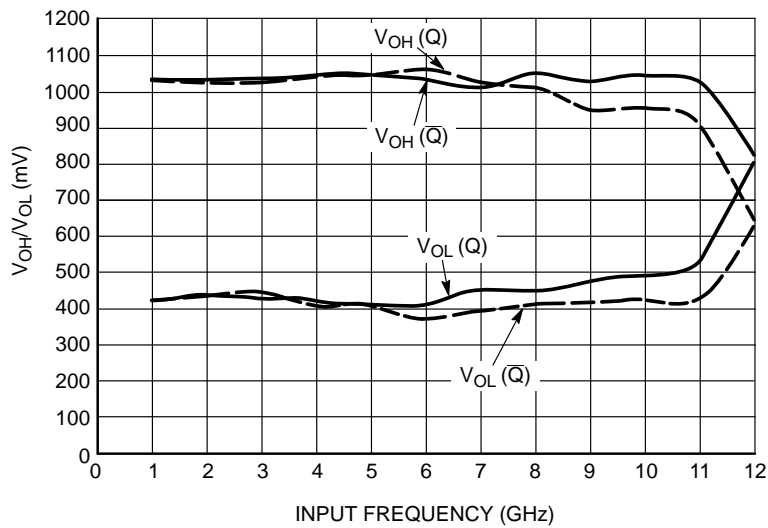
**Figure 7. Output Voltage Amplitude ( $V_{OUTPP}$ ) / RMS Jitter vs. Input Frequency ( $f_{in}$ ) for DIV/2 Mode ( $V_{CC} - V_{EE} = 2.5\text{ V}$  @  $25^\circ\text{C}$ )**

\*When an output level of 400 mV is desired and  $V_{CC} - V_{EE} > 3.0\text{ V}$ , a  $2\text{ k}\Omega$  resistor should be connected from OLS to  $V_{EE}$ .

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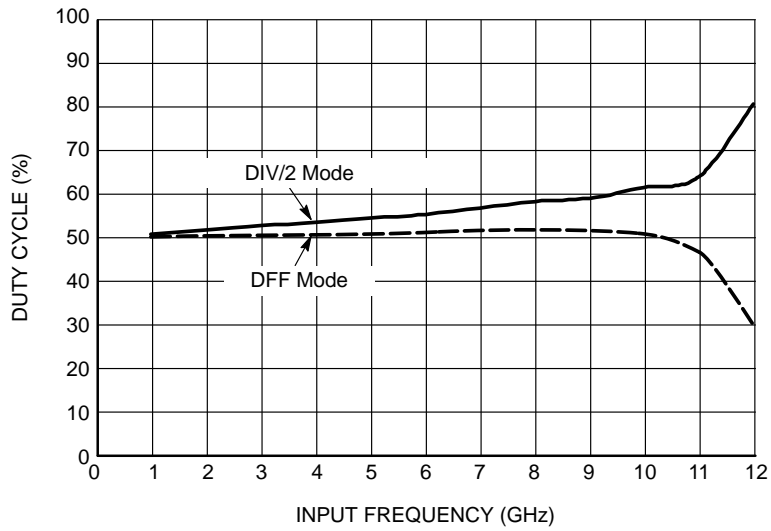


**Figure 8.  $V_{OH}/V_{OL}$  (Q/ $\bar{Q}$ ) vs. Input Frequency ( $f_{in}$ ) for DFF Mode**  
( $V_{CC} - V_{EE} = 3.3$  V @ 25°C and OLS =  $V_{CC} - 0.8$  V, OLS = FLOAT)

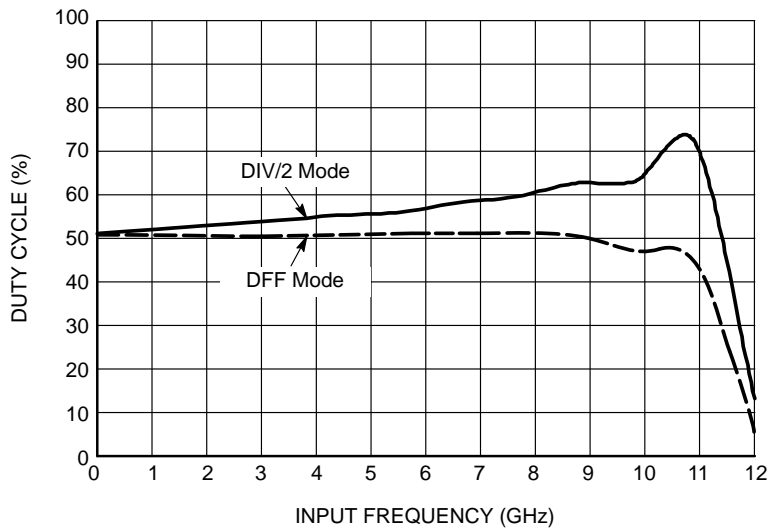


**Figure 9.  $V_{OH}/V_{OL}$  (Q/ $\bar{Q}$ ) vs. Input Frequency ( $f_{in}$ ) for DIV/2 Mode**  
( $V_{CC} - V_{EE} = 3.3$  V @ 25°C and OLS =  $V_{CC} - 0.8$  V, OLS = FLOAT)

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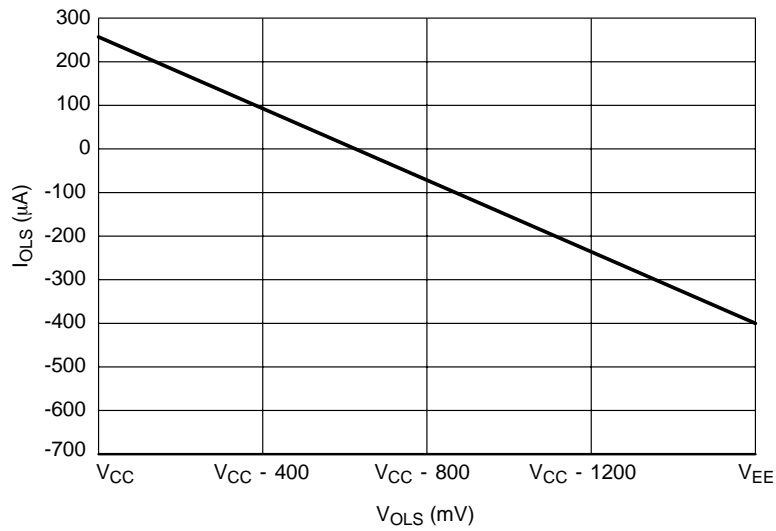


**Figure 10. Duty Cycle % vs. Input Frequency ( $f_{in}$ )**  
 ( $V_{CC} - V_{EE} = 3.3\text{ V @ } 25^{\circ}\text{C}$ )

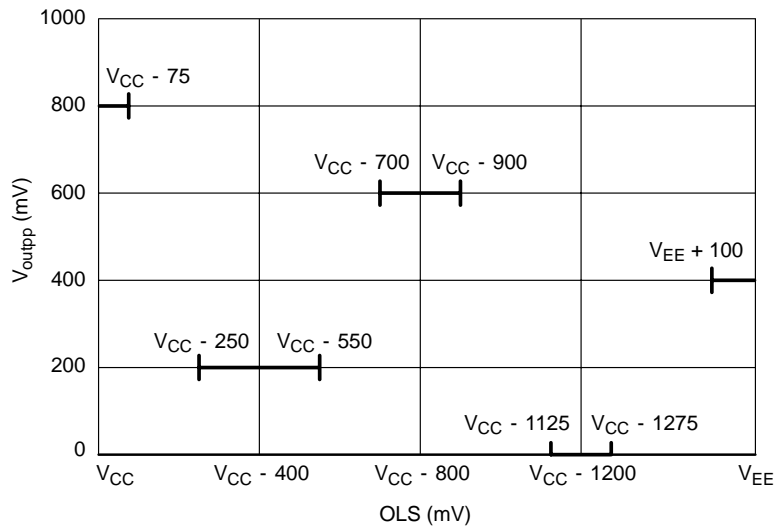


**Figure 11. Duty Cycle % vs. Input Frequency ( $f_{in}$ )**  
 ( $V_{CC} - V_{EE} = 2.5\text{ V @ } 70^{\circ}\text{C}$ )

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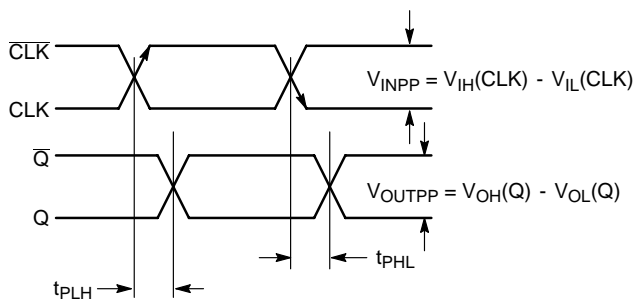
**Figure 12. Typical OLS Input Current vs. OLS Input Voltage**  
( $V_{CC} - V_{EE} = 3.3$  V @ 25°C)



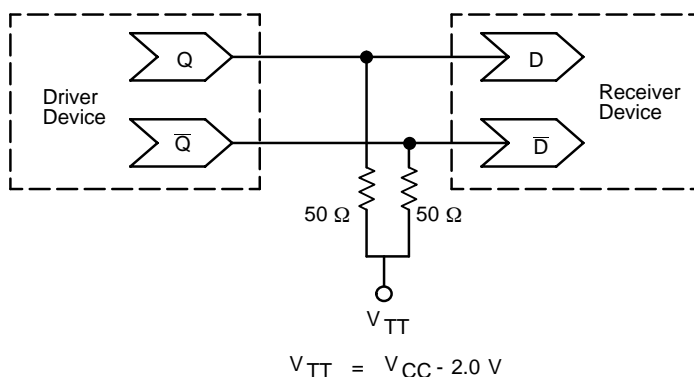
**Figure 13. OLS Operating Area**



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**Figure 14. AC Reference Measurement**



**Figure 15. Typical Termination for Output Driver and Device Evaluation**  
 (Refer to Application Note AND8020 - Termination of ECL Logic Devices)

**NBSG53A**

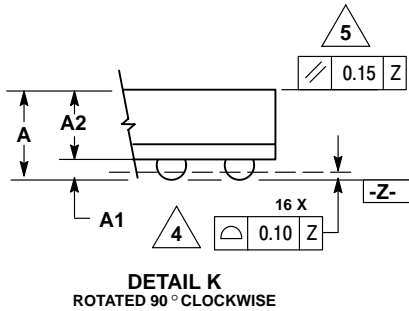
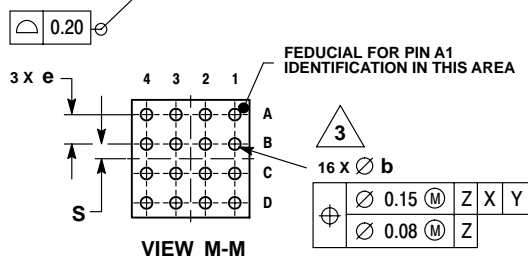
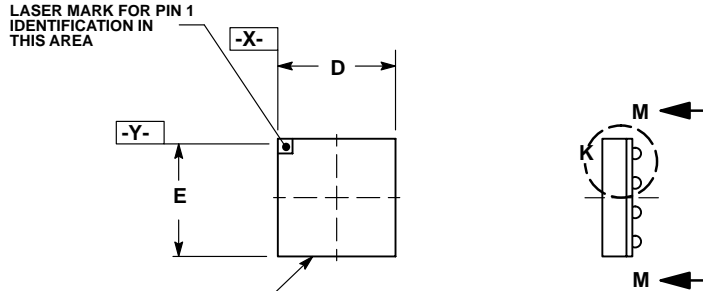
**PACKAGE DIMENSIONS**

**FCBGA-16  
BA SUFFIX**

PLASTIC 4 X 4 (mm) BGA FLIP CHIP PACKAGE

CASE 489-01

ISSUE O



NOTES:

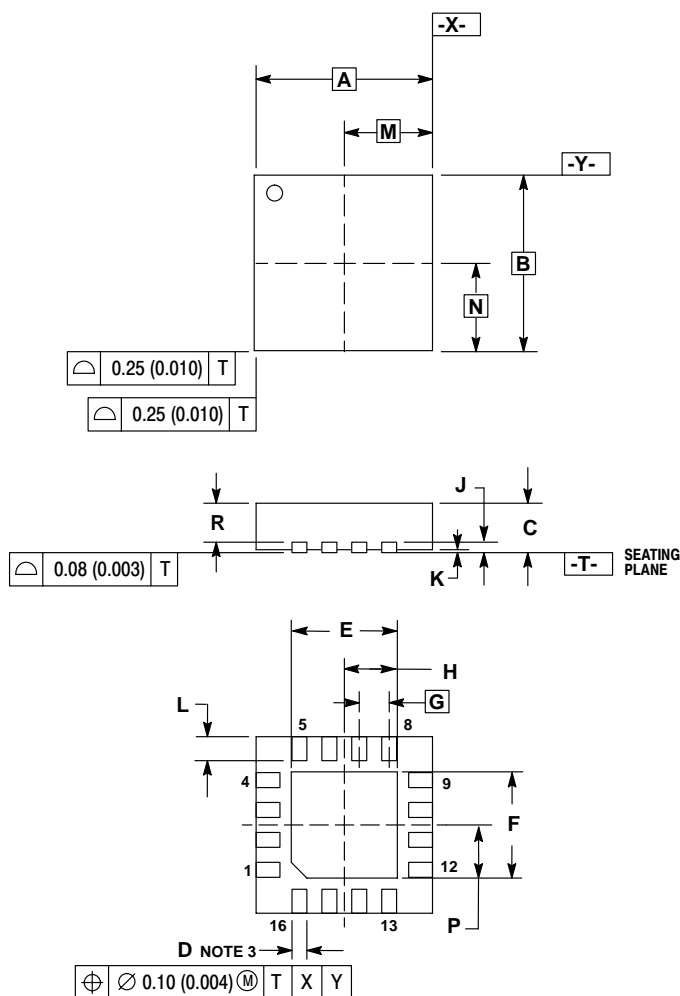
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

DIM	MILLIMETERS	
	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

## NBSG53A

### PACKAGE DIMENSIONS

16 PIN QFN  
MN SUFFIX  
CASE 485G-01  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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