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LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

LMH6574 4:1 High Speed Video Multiplexer

1 Features

- 500 MHz, 500 mV –3 dB Bandwidth, $A_V = 2$
- 400 MHz, 2 V_{PP} –3 dB Bandwidth, $A_V = 2$
- 8 ns Channel Switching Time
- 70 dB Channel to Channel Isolation at 10 MHz
- 0.02%, 0.05° Diff. Gain, Phase
- 0.1 dB Gain Flatness to 150 MHz
- 2200 V/μs Slew Rate
- Wide Supply Voltage Range: 6 V (± 3 V) to 12 V (± 6 V)
- –68 dB HD2 at 5 MHz
- –84 dB HD3 at 5 MHz

2 Applications

- Video Router
- Multi Input Video Monitor
- Instrumentation / Test Equipment
- Receiver IF Diversity Switch
- Multi Channel A/D Driver
- Picture in Picture Video Switch

3 Description

The LMH6574 is a high-performance analog multiplexer optimized for professional grade video and other high fidelity high bandwidth analog applications. The output amplifier selects any one of four buffered input signals based on the state of the two address bits. The LMH6574 provides a 400-MHz bandwidth at 2 V_{PP} output signal levels. Multimedia and high definition television (HDTV) applications can benefit from the LMH6574 0.1 dB bandwidth of 150 MHz and its 2200 V/μs slew rate.

The LMH6574 supports composite video applications with its 0.02% and 0.05° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75-Ω load. An 80-mA linear output current is available for driving multiple video load applications.

The LMH6574 gain is set by external feedback and gain set resistors for maximum flexibility.

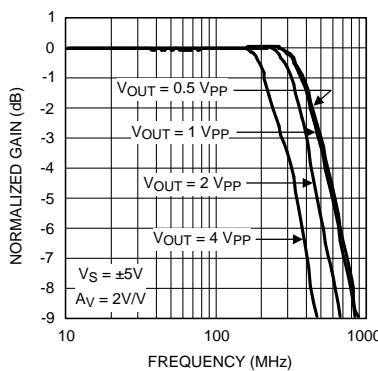
The LMH6574 is available in the 14-pin SOIC package.

Device Information⁽¹⁾

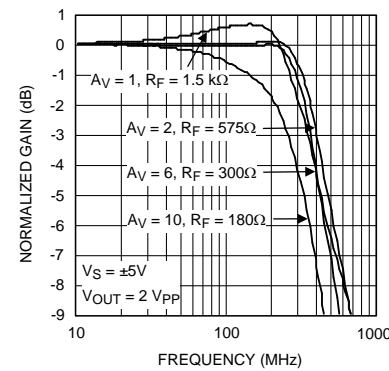
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6574	SOIC (14)	8.65 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Frequency Response vs. V_{OUT}



Frequency Response vs. Gain



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

Table of Contents

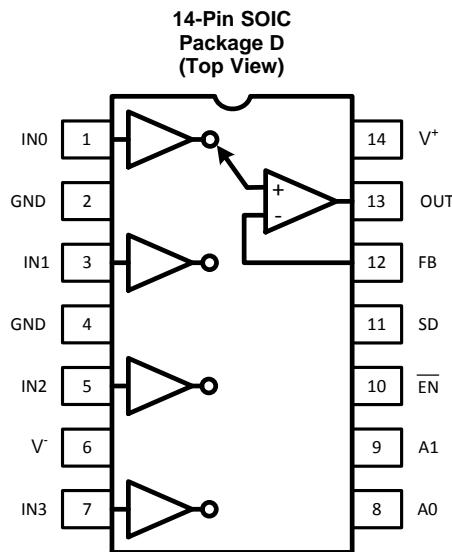
1	Features	1	
2	Applications	1	
3	Description	1	
4	Revision History	2	
5	Pin Configuration and Functions	3	
6	Specifications	4	
6.1	Absolute Maximum Ratings	4	
6.2	ESD Ratings	4	
6.3	Recommended Operating Conditions	4	
6.4	Thermal Information	4	
6.5	Electrical Characteristics $\pm 5V$	5	
6.6	Electrical Characteristics $\pm 3.3V$	7	
6.7	Typical Performance Characteristics	8	
7	Application and Implementation	13	
7.1	Application Information	13	
7.2	Typical Application	13	
8	Power Supply Recommendations	20	
8.1	Power Dissipation	20	
9	Layout	20	
9.1	Layout Guidelines	20	
10	Device and Documentation Support	21	
10.1	Documentation Support	21	
10.2	Trademarks	21	
10.3	Electrostatic Discharge Caution	21	
10.4	Glossary	21	
11	Mechanical, Packaging, and Orderable Information	21	

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2012) to Revision D	Page
• Added, updated, or revised the following sections: <i>Pin Configuration and Functions</i> , <i>Specifications</i> , <i>Application and Implementation</i> , <i>Power Supply Recommendations</i> , <i>Layout</i> , <i>Device and Documentation Support</i> , and <i>Mechanical, Packaging, and Orderable Information</i>	1
• Revised text in <i>Multiplexer Expansion</i> section. Added Figure 29 , Figure 30 , and Figure 31	15

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN0	I	Input Channel 0
2	GND	—	Ground
3	IN1	I	Input Channel 1
4	GND	—	Ground
5	IN2	I	Input Channel 2
6	V ⁻	I	V ⁻ Supply
7	IN3	I	Input Channel 3
8	A0	I	Select Pin A0
9	A1	I	Select Pin A1
10	EN	I	Enable
11	SD	I	Shutdown
12	FB	I	Feedback
13	OUT	O	Output
14	V ⁺	I	V ⁺ Supply

Truth Table

A1	A0	EN	SD	OUT
1	1	0	0	CH 3
1	0	0	0	CH 2
0	1	0	0	CH 1
0	0	0	0	CH 0
X	X	1	0	Disable
X	X	X	1	Shutdown

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

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6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Supply Voltage ($V^+ - V^-$)			13.2	V
$I_{OUT}^{(3)}$			130	mA
Signal & Logic Input Pin Voltage			$\pm(V_S+0.6)$	V
Signal & Logic Input Pin Current			±20	mA
Maximum Junction Temperature			+150	°C
Storage Temperature		-65	+150	°C
Soldering Information	Infrared or Convection (20 sec)		235	°C
	Wave Soldering (10 sec)		260	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the [Electrical Characteristics ±5V](#) tables
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the [Power Dissipation](#) for more details. A short circuit condition should be limited to 5 seconds or less.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge ⁽¹⁾	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾	±2000
		Machine model (MM)	

- (1) Human Body model, 1.5 kΩ in series with 100 pF. Machine model, 0 Ω in series with 200 pF.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	NOM	MAX	UNIT
Operating Temperature	-40		85	°C
Supply Voltage	6		12	V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the [Electrical Characteristics ±5V](#) tables

6.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	D	UNIT
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	40	

- (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report, [SPRA953](#).

6.5 Electrical Characteristics $\pm 5V$

$V_S = \pm 5V$, $R_L = 100\Omega$, $A_V = 2V/V$, $R_F = 575\Omega$, $T_J = 25^\circ C$, Unless otherwise specified.

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE					
SSBW	-3 dB Bandwidth $V_{OUT} = 0.5V_{PP}$		500		MHz
LSBW	-3 dB Bandwidth $V_{OUT} = 2V_{PP}$		400		MHz
.1 dBBW	0.1 dB Bandwidth $V_{OUT} = 0.25V_{PP}$		150		MHz
DG	Differential Gain $R_L = 150\Omega$, $f = 4.43\text{ MHz}$		0.02%		
DP	Differential Phase $R_L = 150\Omega$, $f = 4.43\text{ MHz}$		0.05		deg
XTLK	Channel to Channel Crosstalk All Hostile, 5 MHz		-85		dB
TIME DOMAIN RESPONSE					
TRS	Channel to Channel Switching Time Logic Transition to 90% Output		8		ns
	Enable and Disable Times Logic Transition to 90% or 10% Output		10		ns
TRL	Rise and Fall Time 4-V Step		2.4		ns
TSS	Settling Time to 0.05% 2-V Step		17		ns
OS	Overshoot 2-V Step		5%		
SR	Slew Rate 4-V Step		2200		V/ μ s
DISTORTION					
HD2	2 nd Harmonic Distortion $2V_{PP}$, 5 MHz		-68		dBc
HD3	3 rd Harmonic Distortion $2V_{PP}$, 5 MHz		-84		dBc
IMD	3 rd Order Intermodulation Products 10 MHz, Two Tones $2V_{PP}$ at Output		-80		dBc
EQUIVALENT INPUT NOISE					
VN	Voltage >1 MHz, Input Referred		5		nV/ $\sqrt{\text{Hz}}$
ICN	Current >1 MHz, Input Referred		5		pA/ $\sqrt{\text{Hz}}$
STATIC, DC PERFORMANCE					
CHGM	Channel to Channel Gain Difference DC, Difference in Gain Between Channels	$\pm 0.005\%$ $-40^\circ C \leq T_J \leq 85^\circ C$	$\pm 0.032\%$ $\pm 0.035\%$		
VIO	Input Offset Voltage ⁽²⁾ $V_{IN} = 0V$	1 $-40^\circ C \leq T_J \leq 85^\circ C$	± 20 ± 25		mV
DVIO	Offset Voltage Drift		30		$\mu\text{V}/^\circ C$
IBN	Input Bias Current ⁽²⁾⁽³⁾ $V_{IN} = 0V$	-3 $-40^\circ C \leq T_J \leq 85^\circ C$	± 5 ± 5.6		μA
DIBN	Bias Current Drift		11		$\text{nA}/^\circ C$
	Inverting Input Bias Current Pin 12, Feedback Point, $V_{IN} = 0V$	-7 $-40^\circ C \leq T_J \leq 85^\circ C$	± 10 ± 13		
PSRR	Power Supply Rejection Ratio ⁽²⁾ DC, Input Referred	47 $-40^\circ C \leq T_J \leq 85^\circ C$	54 45		dB

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See [Application and Implementation](#) for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
- (2) Parameters guaranteed by electrical testing at $25^\circ C$.
- (3) Positive Value is current into device.

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

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Electrical Characteristics $\pm 5V$ (continued)

$V_S = \pm 5V$, $R_L = 100\Omega$, $A_V = 2V/V$, $R_F = 575\Omega$, $T_J = 25^\circ C$, Unless otherwise specified.

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
ICC Supply Current ⁽²⁾	No Load			13	16
		-40°C ≤ T_J ≤ 85°C		18	mA
Supply Current Disabled ⁽²⁾	$\overline{ENABLE} > 2V$			4.7	5.8
		-40°C ≤ T_J ≤ 85°C		5.9	mA
Supply Current Shutdown	SHUTDOWN > 2V			1.8	2.5
		-40°C ≤ T_J ≤ 85°C		2.6	mA
VIH Logic High Threshold ⁽²⁾	Select & Enable Pins (SD & \overline{EN})		2.0		V
VIL Logic Low Threshold ⁽²⁾	Select & Enable Pins (SD & \overline{EN})			0.8	V
IiL Logic Pin Input Current Low ⁽³⁾	Logic Input = 0V Select & Enable Pins (SD & \overline{EN})		-2.9	-1	μA
		-40°C ≤ T_J ≤ 85°C	-8.5		
IiH Logic Pin Input Current High ⁽³⁾	Logic Input = 2.0V, Select & Enable Pins (SD & \overline{EN})			47	68
		-40°C ≤ T_J ≤ 85°C		72.5	μA

MISCELLANEOUS PERFORMANCE

RIN+	Input Resistance		5	kΩ	
CIN	Input Capacitance		0.8	pF	
ROUT	Output Resistance	Output Active, (\overline{EN} and SD < 0.8V)	0.04	Ω	
ROUT	Output Resistance	Output Disabled, (\overline{EN} or SD > 2V)	3000	Ω	
COUT	Output Capacitance	Output Disabled, (\overline{EN} or SD > 2V)	3.1	pF	
VO	No Load		±3.54	±3.7	
		-40°C ≤ T_J ≤ 85°C	±3.53	V	
VOL	$R_L = 100\Omega$		±3.18	±3.5	
		-40°C ≤ T_J ≤ 85°C	±3.17	V	
CMIR	Input Voltage Range		±2.5	±2.6	
IO Linear Output Current ⁽²⁾⁽³⁾	$V_{IN} = 0V$		+60		
			-70		
		-40°C ≤ T_J ≤ 85°C	+50	±80	
		-40°C ≤ T_J ≤ 85°C	-60	mA	
ISC	Short Circuit Current ⁽⁴⁾	$V_{IN} = \pm 2V$, Output Shorted to Ground		±230	mA

- (4) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the [Power Dissipation](#) for more details. A short circuit condition should be limited to 5 seconds or less.

6.6 Electrical Characteristics $\pm 3.3V$

$V_S = \pm 3.3V$, $R_L = 100\Omega$, $A_V = 2V/V$, $R_F = 575\Omega$; Unless otherwise specified.

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT
FREQUENCY DOMAIN PERFORMANCE					
SSBW -3 dB Bandwidth	$V_{OUT} = 0.5V_{PP}$		475		MHz
LSBW -3 dB Bandwidth	$V_{OUT} = 2.0V_{PP}$		375		MHz
0.1 dBBW 0.1 dB Bandwidth	$V_{OUT} = 0.5V_{PP}$		100		MHz
GFP Peaking	DC to 200 MHz		0.4		dB
XTLK Channel to Channel Crosstalk	All Hostile, $f = 5\text{ MHz}$		-85		dBc
TIME DOMAIN RESPONSE					
TRL Rise and Fall Time	2-V Step		2		ns
TSS Settling Time to 0.05%	2-V Step		20		ns
OS Overshoot	2-V Step		5%		
SR Slew Rate	2-V Step		1400		V/ μ s
DISTORTION					
HD2 2 nd Harmonic Distortion	2 V_{PP} , 10 MHz		-67		dBc
HD3 3 rd Harmonic Distortion	2 V_{PP} , 10 MHz		-87		dBc
STATIC, DC PERFORMANCE					
VIO Input Offset Voltage	$V_{IN} = 0V$		-5		mV
IBN Input Bias Current ⁽²⁾	$V_{IN} = 0V$		-3		μ A
PSRR Power Supply Rejection Ratio	DC, Input Referred		49		dB
ICC Supply Current	No Load		12		mA
VIH Logic High Threshold	Select & Enable Pins (SD & \overline{EN})		1.3		V
VIL Logic Low Threshold	Select & Enable Pins (SD & \overline{EN})		0.4		V
MISCELLANEOUS PERFORMANCE					
RIN+ Input Resistance			5		k Ω
CIN Input Capacitance			0.8		pF
ROUT Output Resistance			0.06		Ω
VO Output Voltage Range	No Load		± 2		V
VOL	$R_L = 100\Omega$		± 1.8		V
CMIR Input Voltage Range			± 1.2		V
IO Linear Output Current	$V_{IN} = 0V$		± 60		mA
ISC Short Circuit Current	$V_{IN} = \pm 1V$, Output Shorted to Ground		± 150		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See [Application and Implementation](#) for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Positive Value is current into device.

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

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6.7 Typical Performance Characteristics

$V_S = \pm 5 V$, $R_L = 100 \Omega$, $A_V = 2$, $R_F = R_G = 575 \Omega$, unless otherwise specified.

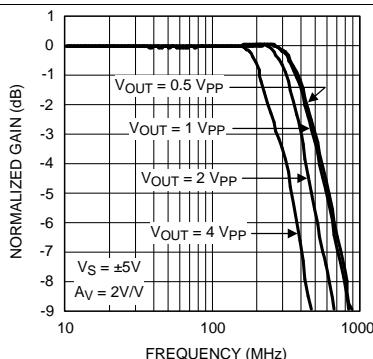


Figure 1. Frequency Response vs. V_{OUT}

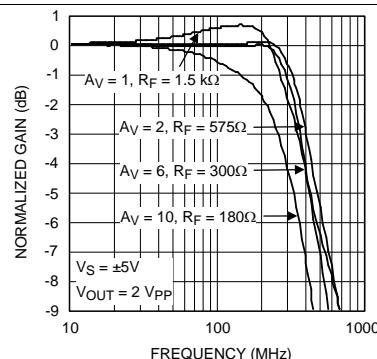


Figure 2. Frequency Response vs. Gain

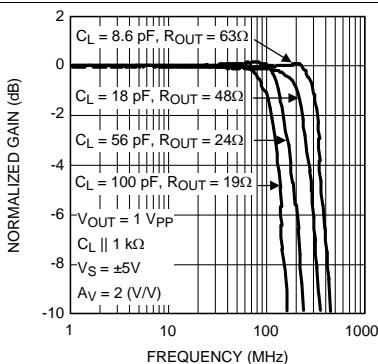


Figure 3. Frequency Response vs. Capacitive Load

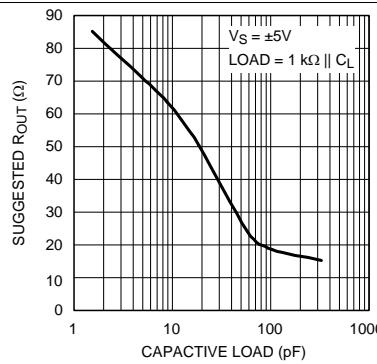


Figure 4. Suggested R_{OUT} vs. Capacitive Load

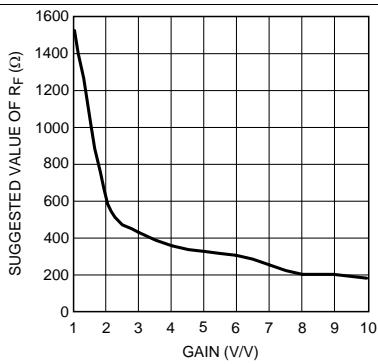


Figure 5. Suggested Value of R_F vs. Gain

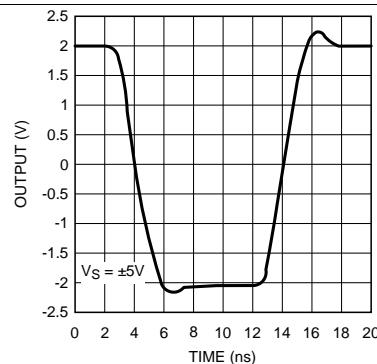


Figure 6. Pulse Response 4V_{PP}

Typical Performance Characteristics (continued)

$V_S = \pm 5 \text{ V}$, $R_L = 100 \Omega$, $A_V = 2$, $R_F = R_G = 575 \Omega$, unless otherwise specified.

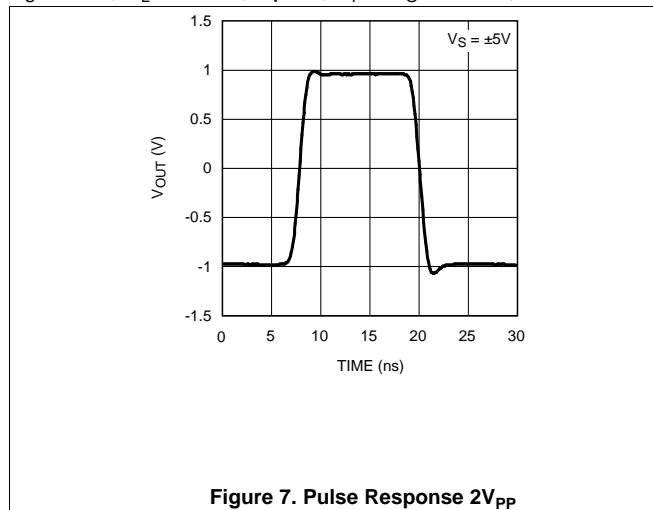


Figure 7. Pulse Response 2V_{PP}

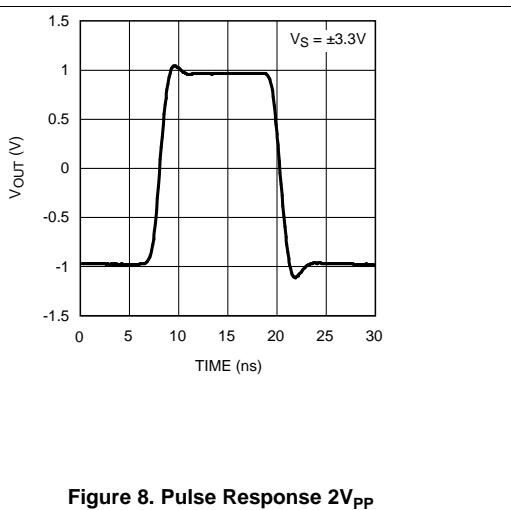


Figure 8. Pulse Response 2V_{PP}

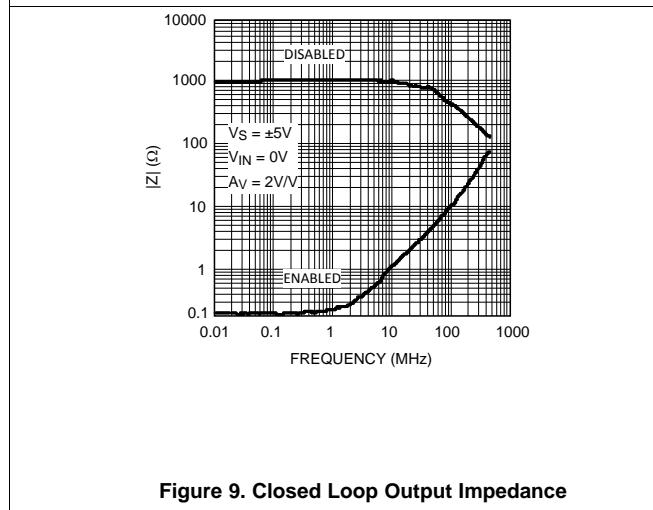


Figure 9. Closed Loop Output Impedance

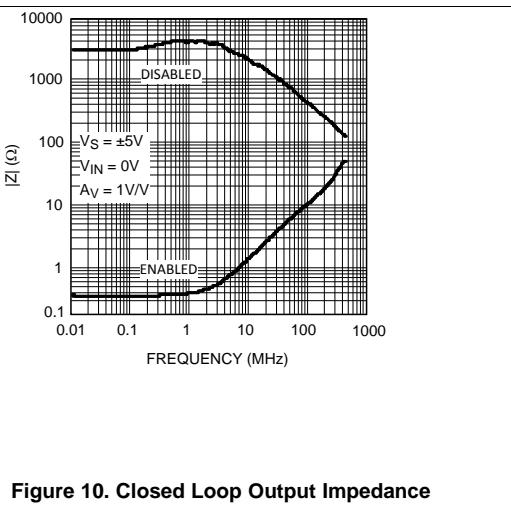


Figure 10. Closed Loop Output Impedance

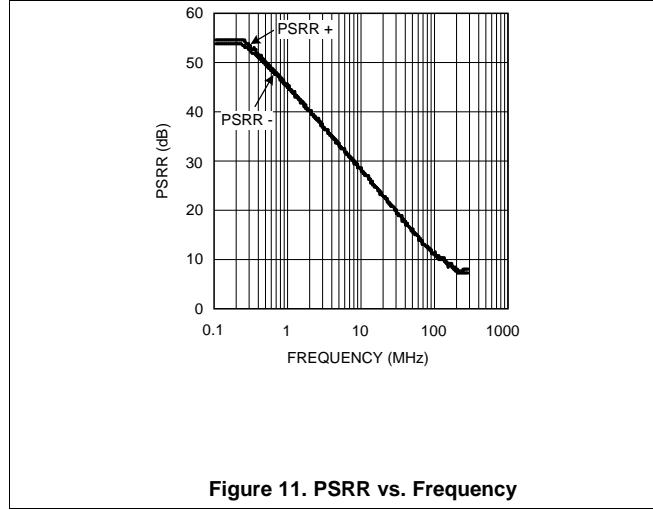


Figure 11. PSRR vs. Frequency

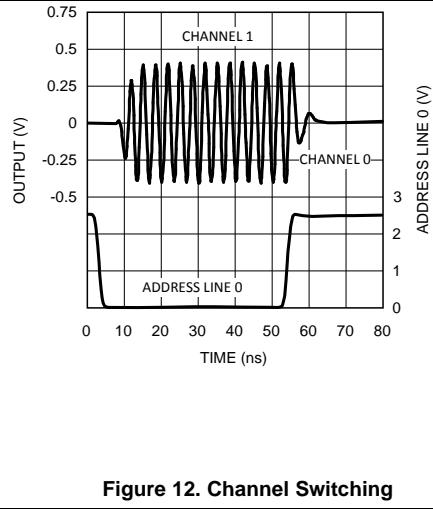


Figure 12. Channel Switching

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

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Typical Performance Characteristics (continued)

$V_S = \pm 5 \text{ V}$, $R_L = 100 \Omega$, $A_V = 2$, $R_F = R_G = 575 \Omega$, unless otherwise specified.

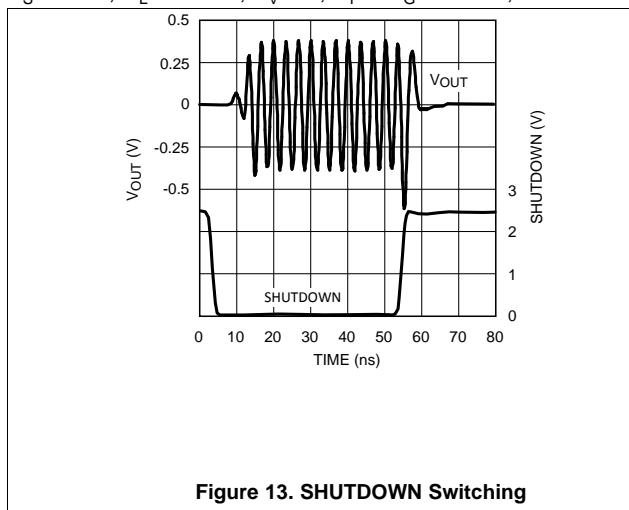


Figure 13. SHUTDOWN Switching

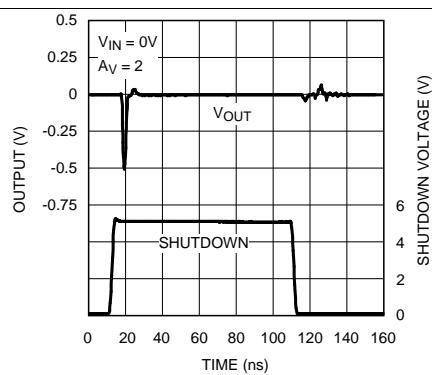


Figure 14. Shutdown Glitch

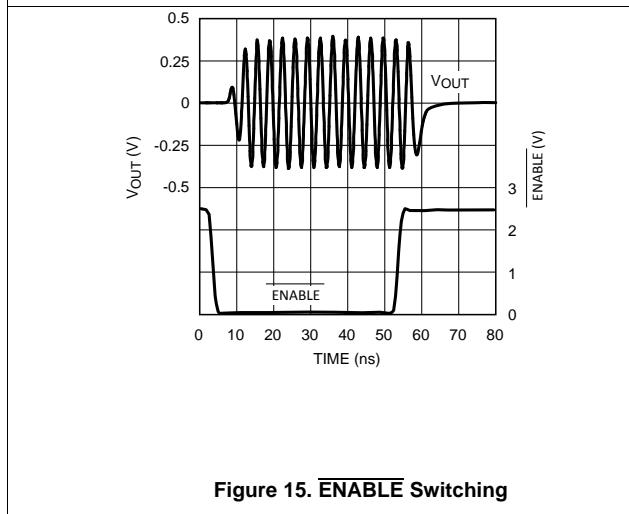


Figure 15. ENABLE Switching

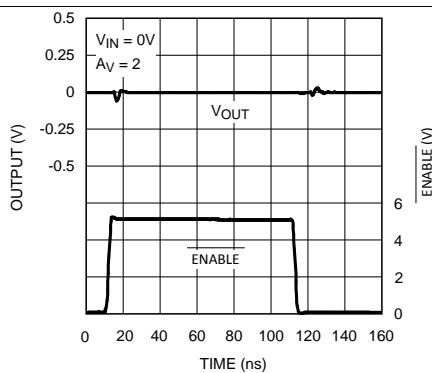


Figure 16. Disable Glitch

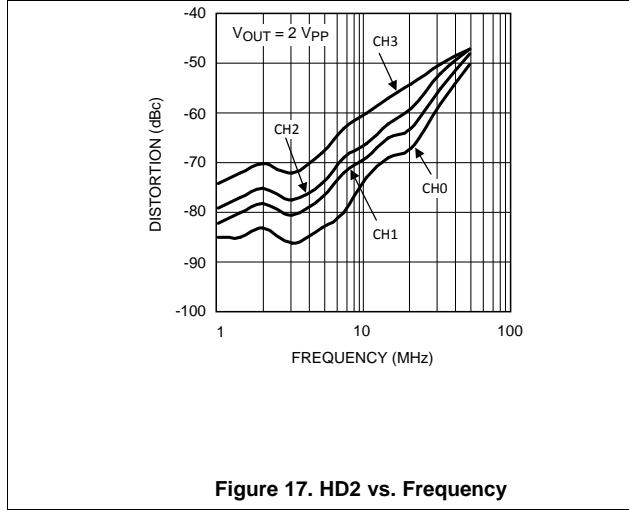


Figure 17. HD2 vs. Frequency

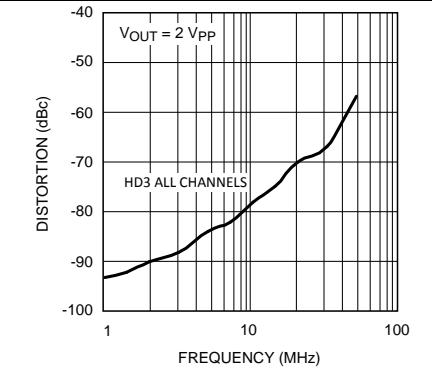


Figure 18. HD3 vs. Frequency

Typical Performance Characteristics (continued)

$V_S = \pm 5 \text{ V}$, $R_L = 100 \Omega$, $A_V = 2$, $R_F = R_G = 575 \Omega$, unless otherwise specified.

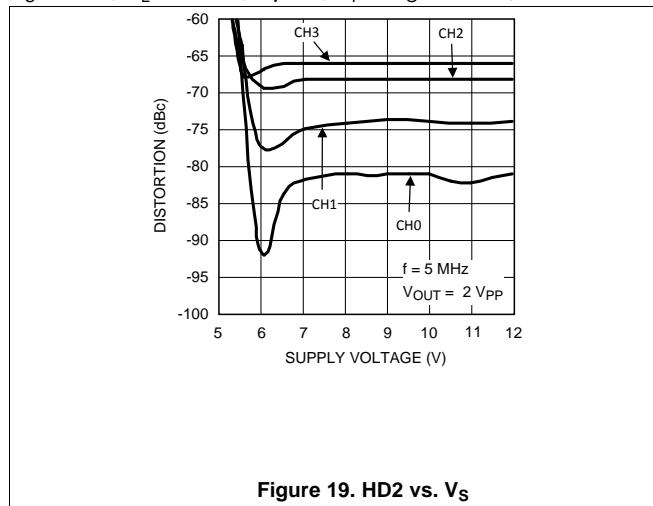


Figure 19. HD2 vs. V_S

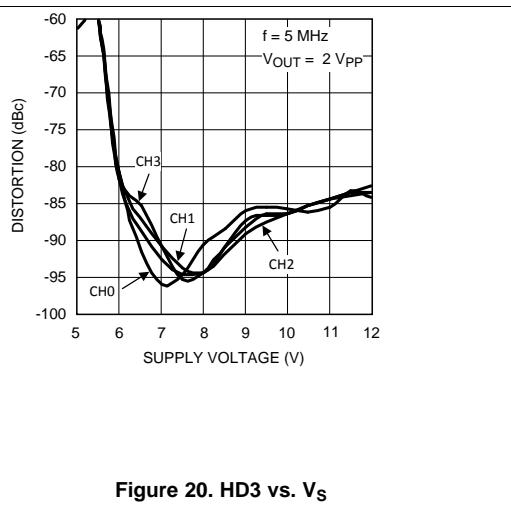


Figure 20. HD3 vs. V_S

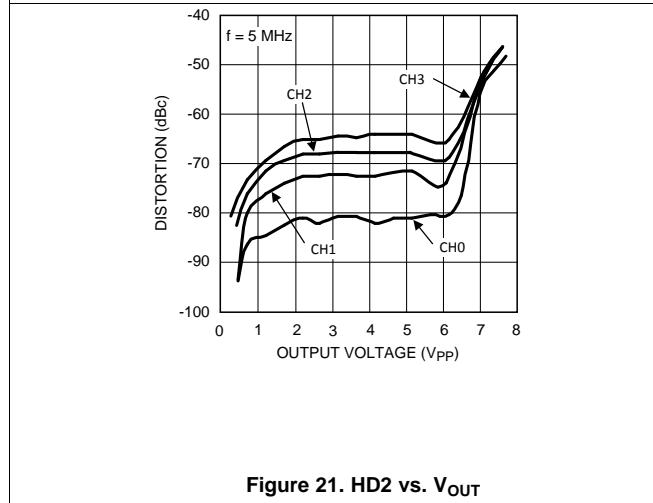


Figure 21. HD2 vs. V_{OUT}

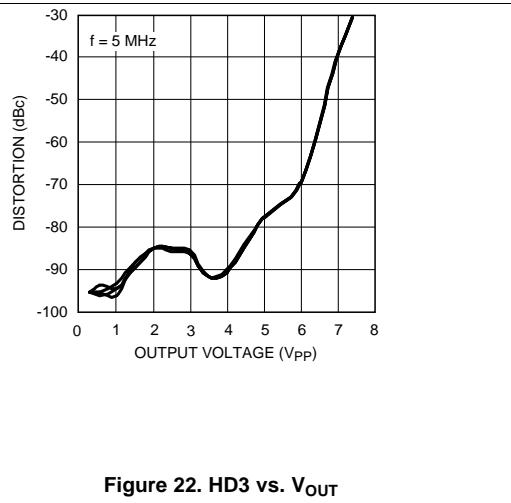


Figure 22. HD3 vs. V_{OUT}

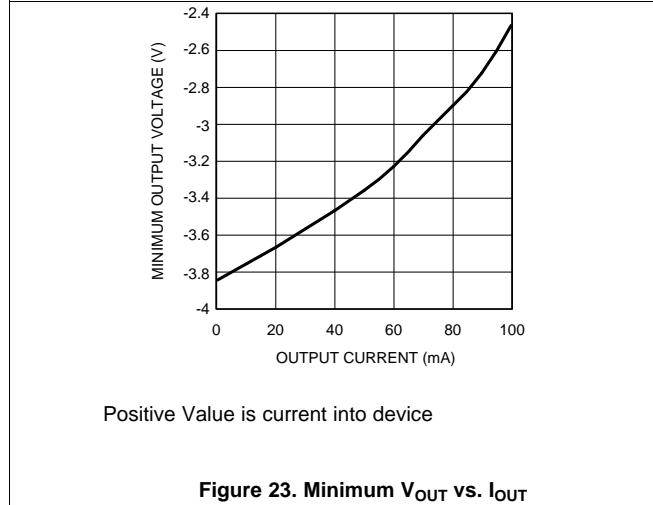


Figure 23. Minimum V_{OUT} vs. I_{OUT}

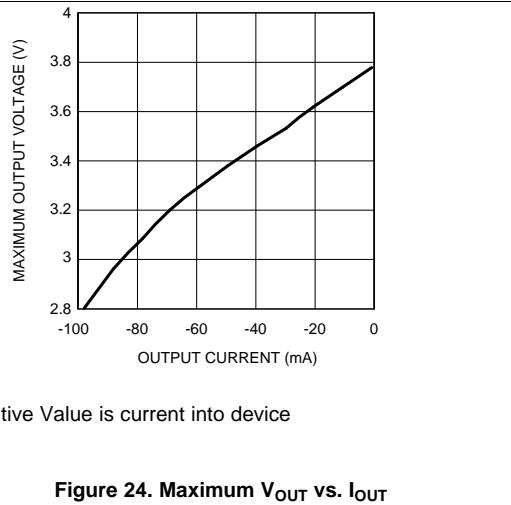


Figure 24. Maximum V_{OUT} vs. I_{OUT}

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

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Typical Performance Characteristics (continued)

$V_S = \pm 5 V$, $R_L = 100 \Omega$, $A_V = 2$, $R_F = R_G = 575 \Omega$, unless otherwise specified.

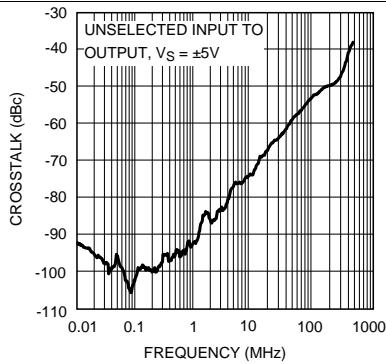


Figure 25. Crosstalk vs. Frequency

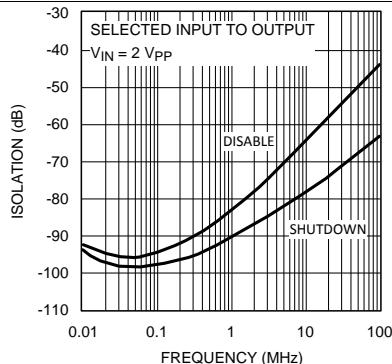


Figure 26. Off Isolation

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The LMH6574 is a high-speed 4:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6574 is ideally suited for switching high resolution, presentation grade video signals. The LMH6574 has no internal ground reference. Single or split supply configurations are both possible. The LMH6574 features very high speed channel switching and disable times. When disabled the LMH6574 output is high impedance making MUX expansion possible by combining multiple devices. See *Multiplexer Expansion*.

7.2 Typical Application

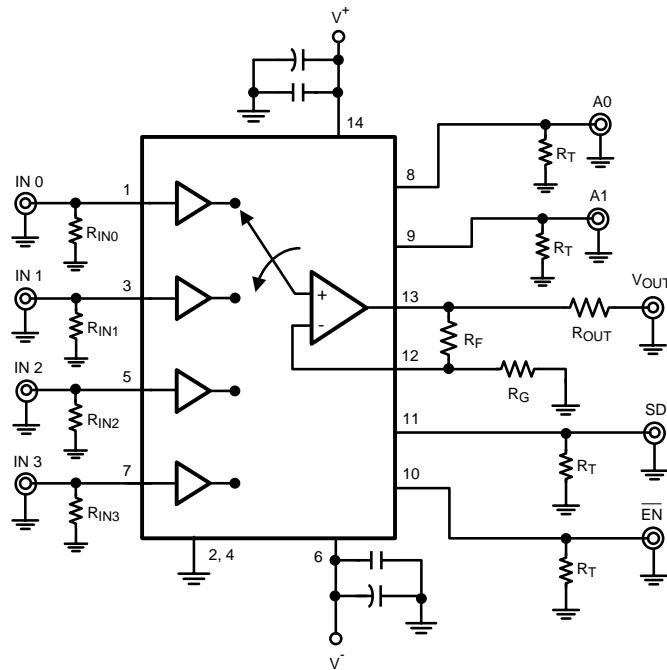


Figure 27. Typical Application

7.2.1 Video Performance

The LMH6574 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 27 shows a typical configuration for driving a 75Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

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Typical Application (continued)

7.2.2 Feedback Resistor Selection

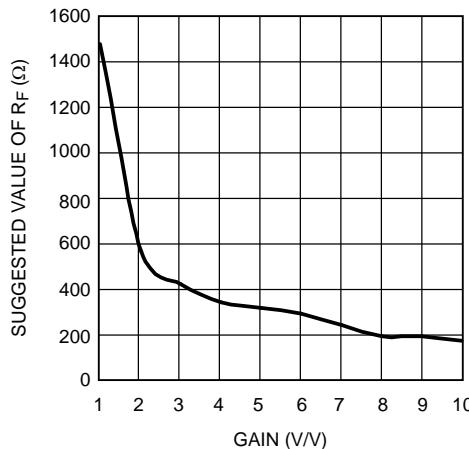


Figure 28. Suggested R_F vs. Gain

The LMH6574 has a current feedback output buffer with gain determined by external feedback (R_F) and gain set (R_G) resistors. With current feedback amplifiers, the closed loop frequency response is a function of R_F . For a gain of 2 V/V, the recommended value of R_F is 575Ω . For other gains see [Figure 28](#). Generally, lowering R_F from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different it is worth some experimentation to find the optimal R_F for a given circuit. For more information see *Current Feedback Loop Gain Analysis and Performance Enhancement*, Application Note OA-13 ([SNOA366](#)), which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 12 is approximately 20Ω . This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6574 will exhibit a “gain bandwidth product” similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 ([SNOA39](#)) to provide additional gain.

7.2.3 SD vs. \overline{EN}

The LMH6574 has both shutdown and disable capability. The shutdown feature affects the entire chip, whereas the disable function only affects the output buffer. When in shutdown mode, minimal power is consumed. The shutdown function is very fast, but causes a very brief spike of about 400 mV to appear on the output. When in shutdown mode the LMH6574 consumes only 1.8 mA of supply current. For maximum input to output isolation use the shutdown function.

The \overline{EN} pin only disables the output buffer which results in a substantially reduced output glitch of only 50 mV. While disabled the chip consumes 4.7 mA, considerably more than when shutdown. This is because the input buffers are still active. For minimal output glitch use the \overline{EN} pin. Also, care should be taken to ensure that, while in the disabled state, the voltage differential between the active input buffer (the one selected by pins A0 and A1) and the output pin stays less than 2V. As the voltage differential increases, input to output isolation decreases. Normally this is not an issue. See [Multiplexer Expansion](#) for further details.

To reduce the output glitch when using the SD pin, switch the \overline{EN} pin at least 10 ns before switching the SD pin. This can be accomplished by using an RC delay circuit between the two pins if only one control signal is available.

Logic inputs "SD" and " \overline{EN} " will revert to the "High", while " A_0 " and " A_1 " will revert to the "Low" state when left floating.

Typical Application (continued)

7.2.4 Multiplexer Expansion

It is possible to use multiple LMH6574 devices to expand the number of inputs that can be selected for output. Figure 29 shows an 8:1 MUX using two LMH6574 devices.

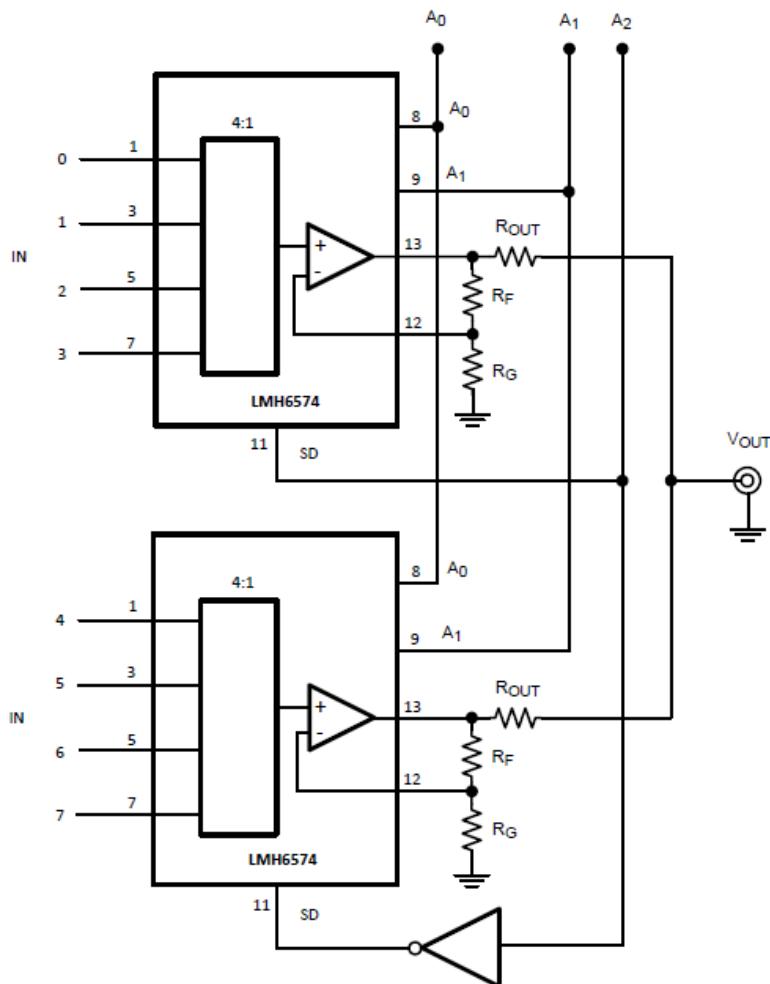


Figure 29. 8:1 MUX Using Two LMH6574 Devices

In such an application, the output settling may be longer than the LMH6574 switching specifications (~20ns), while switching between two separate LMH6574 devices. The switching time limiting factor occurs when one LMH6574 is turned off and another one is turned on, using the SD (shutdown) pin. The output settling time consists of the time needed for the first LMH6574 to enter high impedance state plus the time required for the second LMH6574 output to dissipate the left-over output charge of the first device (limited by the output current capability of the second device) and the time needed to settle to the final voltage value.

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

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Typical Application (continued)

While Figure 29 MUX expansion benefits from more isolation, originating from the parasitic loading of the unselected channels on the selected channel, afforded by individual R_{OUT} on each multiplexer output, this configuration does not produce the fastest transition between individual LMH6574 devices. For the fastest transition, the configuration of Figure 30 can be used where the LMH6574 output pins are all shorted together.

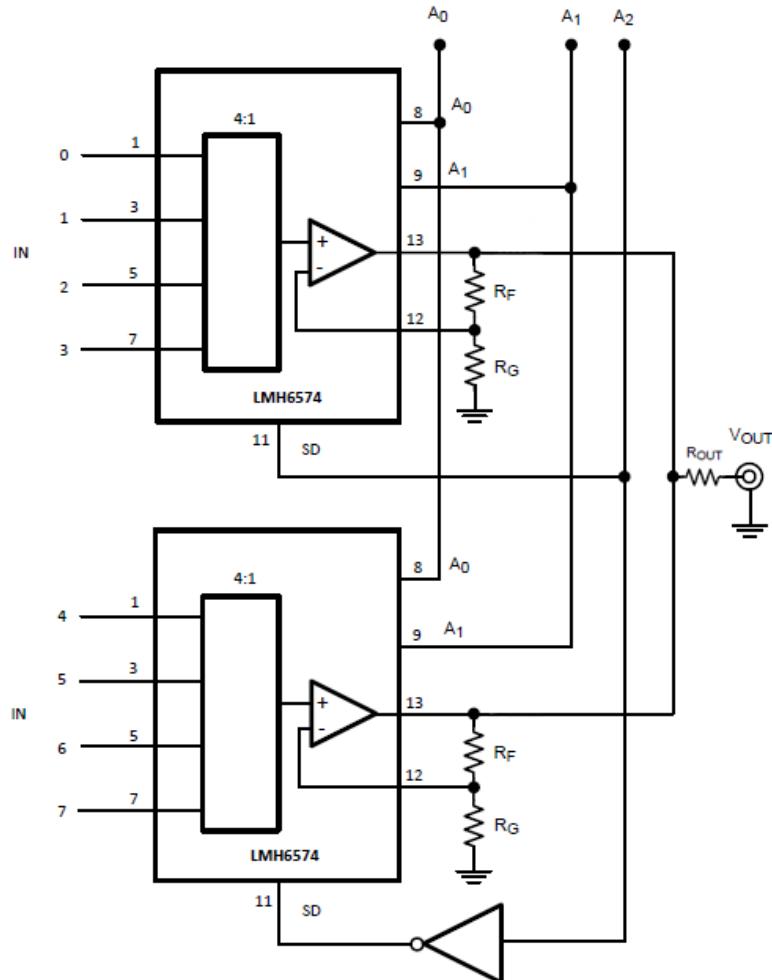


Figure 30. Alternate 8:1 MUX Expansion Schematic (for Faster SD Switching)

Typical Application (continued)

Figure 31 shows typical transition waveforms and shows that SD pin switching settles in less than 145 ns.

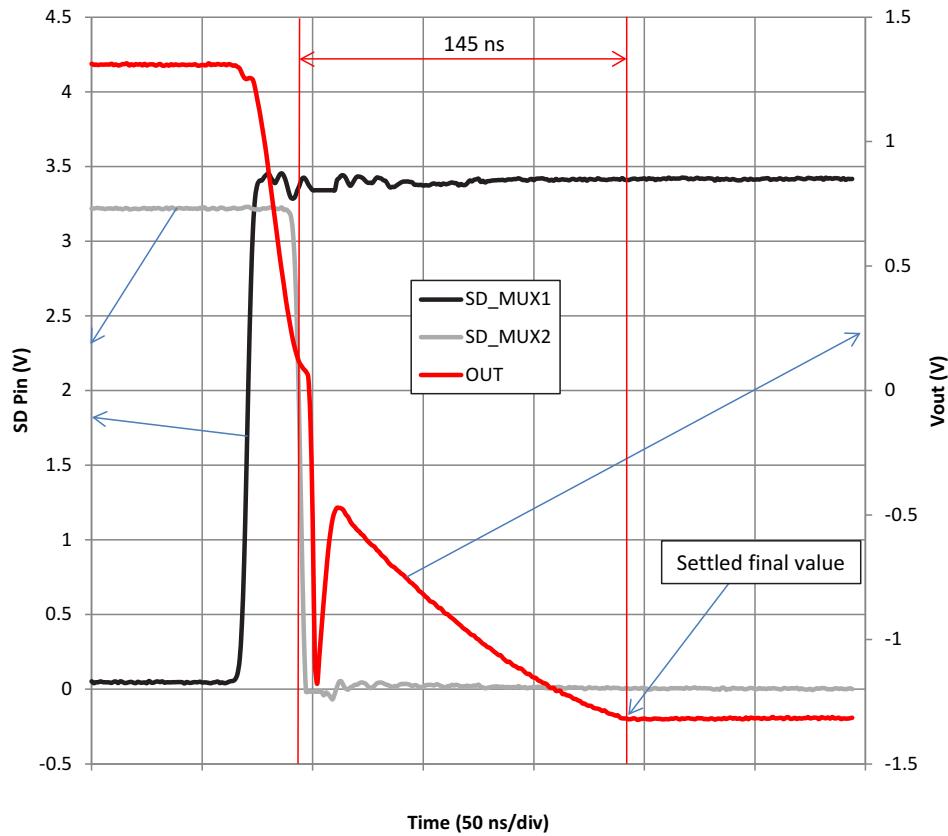


Figure 31. SD Pin Switching Waveform and Output Settling

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device. Figure 32 shows one possible approach to this delay circuit. The delay circuit shown will delay SHUTDOWN's H to L transitions (R1 and C1 decay) but will not delay its L to H transition. R2 should be kept small compared to R1 in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

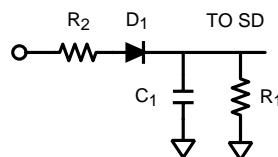


Figure 32. Delay Circuit Implementation

LMH6574

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Typical Application (continued)

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6574's can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in [Figure 33](#) shows how to compensate for this effect. For the 16:1 MUX function shown in [Figure 33](#), the gain error would be about -0.8 dB, or about 9%. In the circuit in [Figure 33](#), resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).

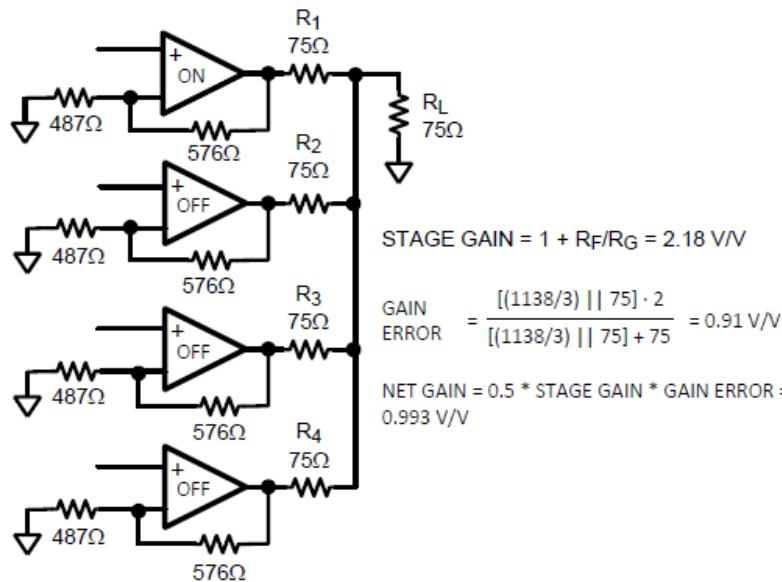


Figure 33. Multiplexer Gain Compensation

NOTE

Disabling of the LMH6574 using the EN pin is not recommended for use when doing multiplexer expansion. While disabled, If the voltage between the selected input and the chip output exceeds approximately 2V the device will begin to enter a soft breakdown state. This will show up as reduced input to output isolation. The signal on the non-inverting input of the output driver amplifier will leak through to the inverting input, and then to the output through the feedback resistor. The worst case is a gain of 1 configuration where the non inverting input follows the active input buffer and (through the feedback resistor) the inverting input follows the voltage driving the output stage. The solution for this is to use shutdown mode for multiplexer expansion.

7.2.5 Other Applications

The LMH6574 could support a multi antenna receiver with up to four separate antennas. Monitoring the signal strength of all 4 antennas and connecting the strongest signal to the final IF stage would provide effective spacial diversity.

For direction finding, the LMH6574 could be used to provide high speed sampling of four separate antennas to a single DSP which would use the information to calculate the direction of the received signal.

Typical Application (continued)

7.2.6 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT} . Figure 34 shows the use of a series output resistor, R_{OUT} , to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 35 provides a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

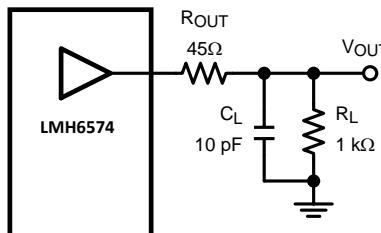


Figure 34. Decoupling Capacitive Loads

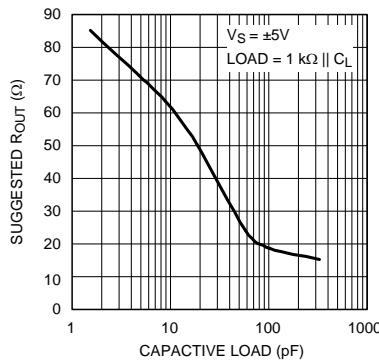


Figure 35. Suggested R_{OUT} vs. Capacitive Load

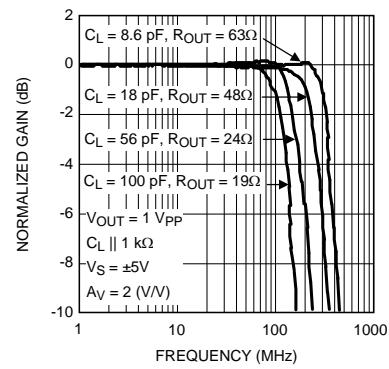


Figure 36. Frequency Response vs. Capacitive Load

7.2.7 ESD Protection

The LMH6574 is protected against electrostatic discharge (ESD) on all pins. The LMH6574 will survive 2000-V Human Body model and 200-V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6574 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

LMH6574

SNCS103D – NOVEMBER 2004 – REVISED DECEMBER 2014

www.ti.com

8 Power Supply Recommendations

8.1 Power Dissipation

The LMH6574 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6574:

1. Calculate the quiescent (no-load) power.

$$P_{AMP} = I_{CC} * (V_S)$$

where

- $V_S = V^+ - V^-$

 (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D (\text{rms}) = \text{rms} ((V_S - V_{OUT}) * I_{OUT})$$

where

- V_{OUT} is the voltage across the external load
 - I_{OUT} is the current through the external load
 - V_S is the total supply voltage
- (2)

3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that the LMH6574 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150^\circ - T_{AMB})/R_{\theta JA}$$

where

- T_{AMB} = Ambient temperature ($^\circ\text{C}$)
 - $R_{\theta JA}$ = Thermal resistance, from junction to ambient, for a given package ($^\circ\text{C}/\text{W}$)
- (3)

For the SOIC package $R_{\theta JA}$ is 130 $^\circ\text{C}/\text{W}$.

9 Layout

9.1 Layout Guidelines

Whenever questions about layout arise, use the evaluation board LMH730276 ([SNOU028](#)) as a guide. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In [Figure 27](#), the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01 μF and 0.1 μF ceramic capacitors for each supply bypass.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For additional information, see the following:

- *Current Feedback Loop Gain Analysis and Performance Enhancement*, Application Note OA-13 ([SNOA366](#))
- *IC Package Thermal Metrics Application Report* ([SPRA953](#))
- *LMH730276 4:1 Multiplexer Evaluation Board* ([SNOU028](#))

10.2 Trademarks

All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6574MA	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85		
LMH6574MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 74MA	Samples
LMH6574MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 74MA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "—" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

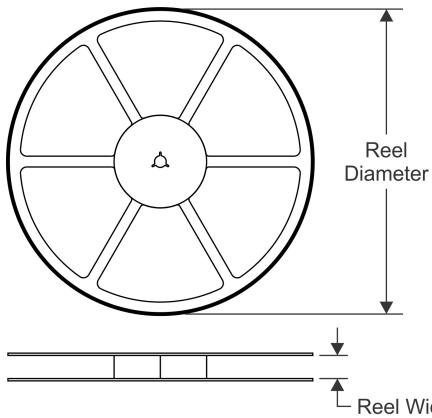
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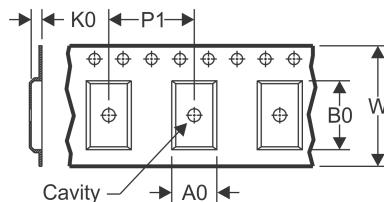
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REEL DIMENSIONS

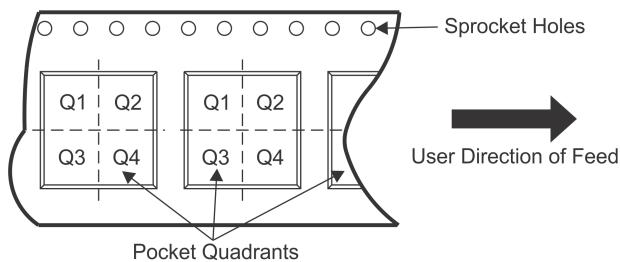


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

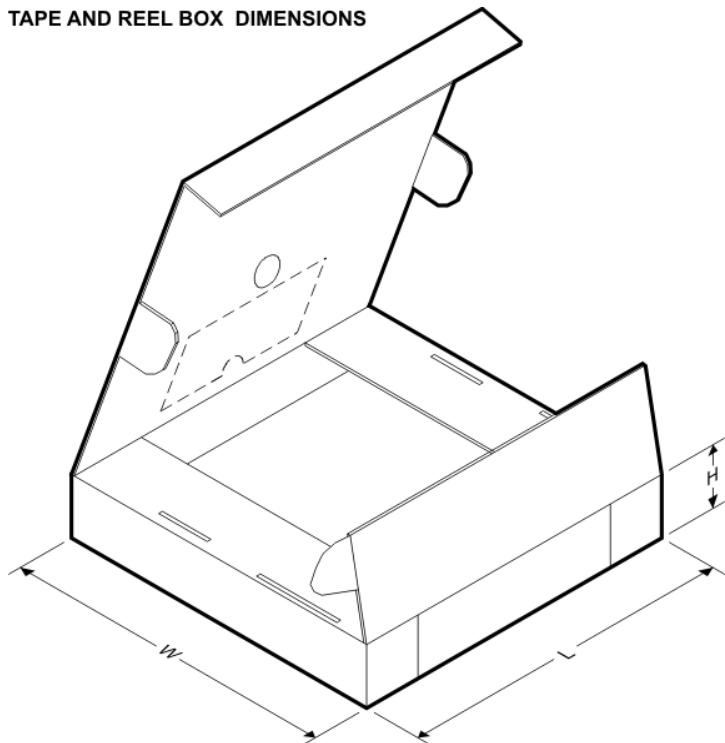
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6574MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



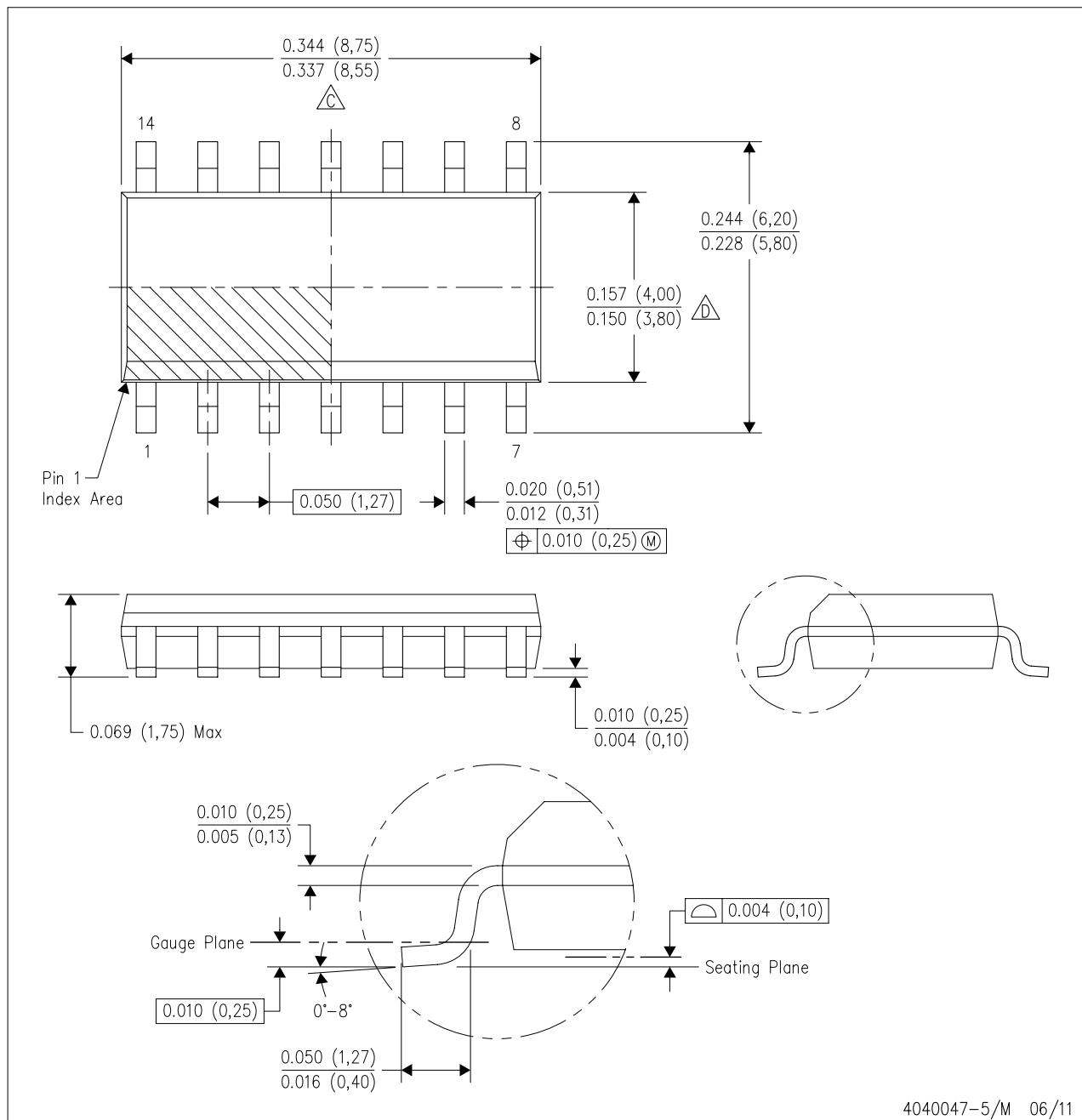
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6574MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

MECHANICAL DATA

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

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