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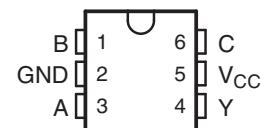
SINGLE-SUPPLY VOLTAGE-LEVEL TRANSLATOR WITH NINE CONFIGURABLE GATE LOGIC FUNCTIONS

 Check for Samples: [SN74AUP1T98](#)

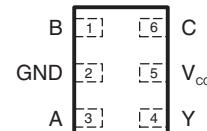
FEATURES

- Available in the Texas Instruments NanoStar™ Packages
- Single-Supply Voltage Translator
- 1.8 V to 3.3 V (at $V_{CC} = 3.3$ V)
- 2.5 V to 3.3 V (at $V_{CC} = 3.3$ V)
- 1.8 V to 2.5 V (at $V_{CC} = 2.5$ V)
- 3.3 V to 2.5 V (at $V_{CC} = 2.5$ V)
- Nine Configurable Gate Logic Functions
- Schmitt-Trigger Inputs Reject Input Noise and Provide Better Output Signal Integrity
- I_{off} Supports Partial-Power-Down Mode With Low Leakage Current (0.5 μ A)
- Very Low Static and Dynamic Power Consumption
- Pb-Free Packages Available: SOT-23 (DBV), SC-70 (DCK), and W CSP (NanoStar)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Related Devices: SN74AUP1T97, SN74AUP1T57, and SN74AUP1T58

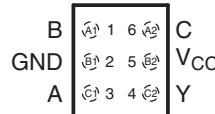
**DBV OR DCK PACKAGE
(TOP VIEW)**



**DRY OR DSF PACKAGE
(TOP VIEW)**



**YFP OR YZP PACKAGE
(TOP VIEW)**



DESCRIPTION

AUP technology is the industry's lowest-power logic technology designed for use in battery-operated or battery backed-up equipment. The SN74AUP1T98 is designed for logic-level translation applications with input switching levels that accept 1.8-V LVC MOS signals, while operating from either a single 3.3-V or 2.5-V V_{CC} supply.

The wide V_{CC} range of 2.3 V to 3.6 V allows the possibility of battery voltage drop during system operation and ensures normal operation between this range.

Schmitt-trigger inputs ($\Delta V_T = 210$ mV between positive and negative input transitions) offer improved noise immunity during switching transitions, which is especially useful on analog mixed-mode designs. Schmitt-trigger inputs reject input noise, ensure integrity of output signals, and allow for slow input signal transition.

The SN74AUP1T98 can be easily configured to perform a required gate function by connecting A, B, and C inputs to V_{CC} or ground (see Function Selection table). Up to nine commonly used logic gate functions can be performed.

I_{off} is a feature that allows for powered-down conditions ($V_{CC} = 0$ V) and is important in portable and mobile applications. When $V_{CC} = 0$ V, signals in the range from 0 V to 3.6 V can be applied to the inputs and outputs of the device. No damage occurs to the device under these conditions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.

The SN74AUP1T98 is designed with optimized current-drive capability of 4 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

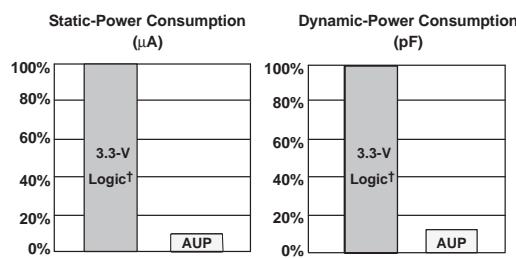
NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

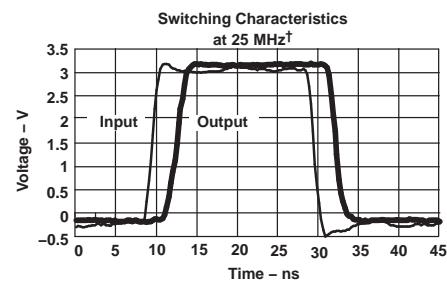
FUNCTION SELECTION TABLE

LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	5
2-input NAND gate	6
2-input NOR gate with one inverted input	7
2-input NAND gate with one inverted input	7
2-input NAND gate with one inverted input	8
2-input NOR gate with one inverted input	8
2-input NOR gate	9
Inverter	10
Noninverted buffer	11



† Single, dual, and triple gates

Figure 1. AUP – The Lowest-Power Family



† AUP1G08 data at $C_L = 15 \text{ pF}$

Figure 2. Excellent Signal Integrity

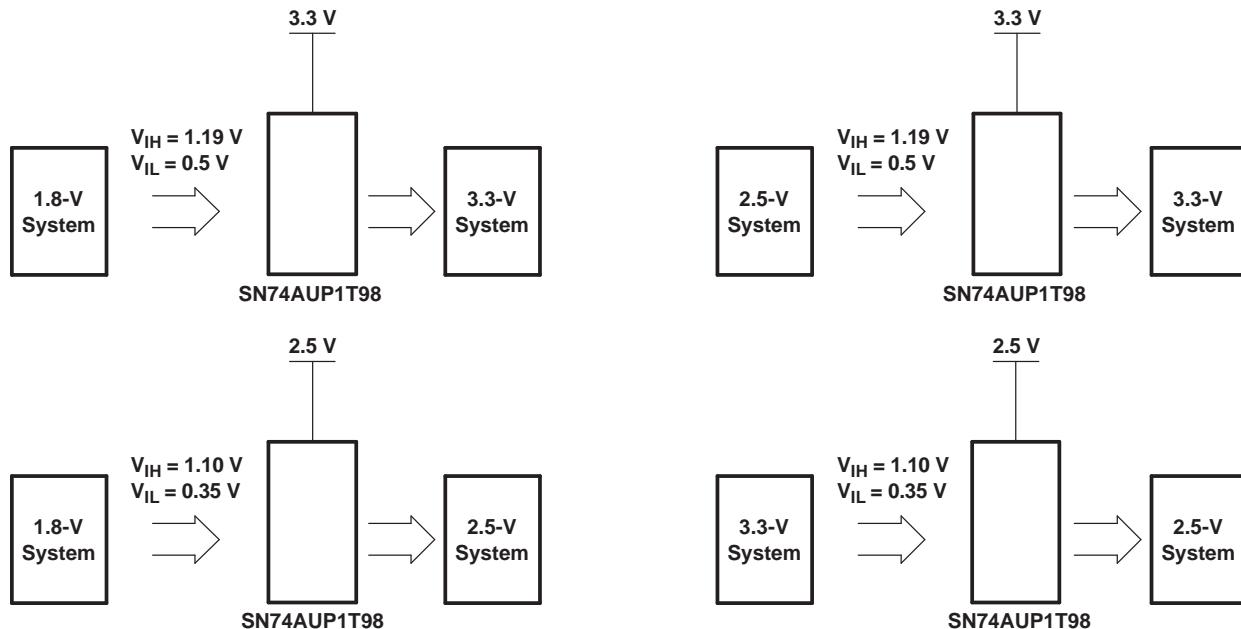


Figure 3. Possible Voltage-Translation Combinations

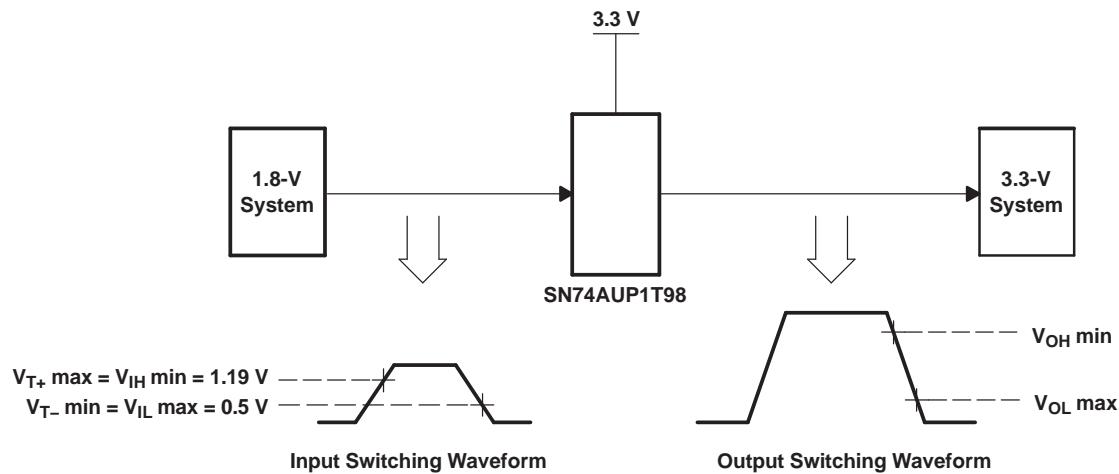
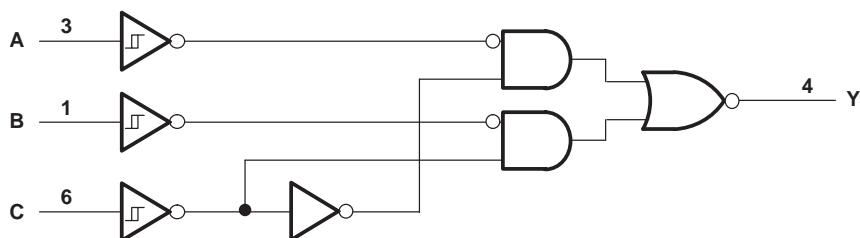


Figure 4. Switching Thresholds for 1.8-V to 3.3-V Translation

FUNCTION TABLE

INPUTS			OUTPUT Y
C	B	A	
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC CONFIGURATIONS

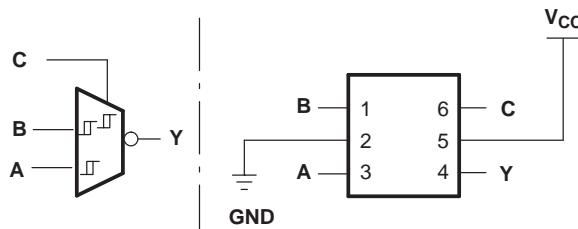


Figure 5. 157+04: 2-to-1 Data Selector With Inverted Output
When C is L, Y = \overline{B}
When C is H, Y = A

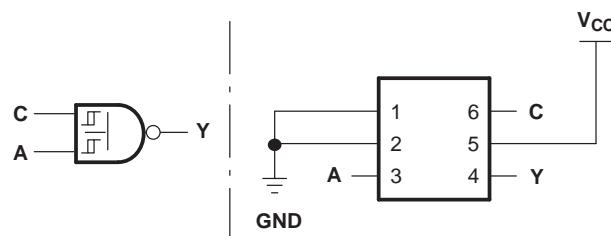
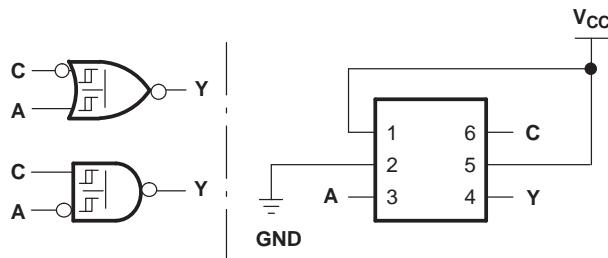
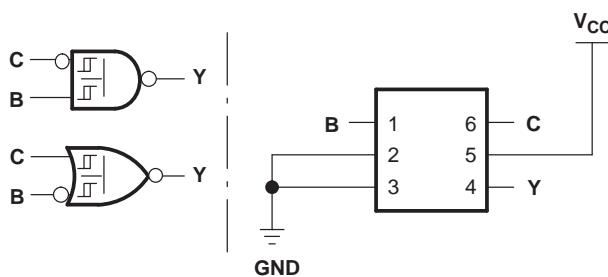


Figure 6. 00: 2-Input NAND Gate



**Figure 7. 14+02/14+08: 2-Input NOR Gate With One Inverted Input
2-Input NAND Gate With One Inverted Input**



**Figure 8. 14+00/14+32: 2-Input NAND Gate With One Inverted Input
2-Input NOR Gate With One Inverted Input**

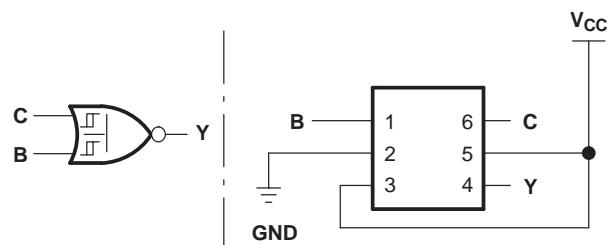


Figure 9. 32: 2-Input NOR Gate

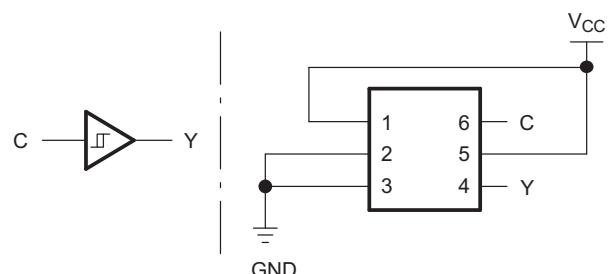


Figure 10. 17/34: Noninverted Buffer

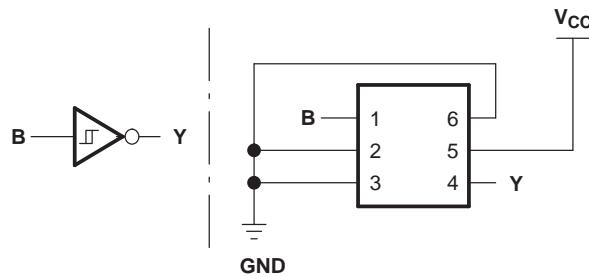


Figure 11. 04/14: Inverter

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 20	mA
	Continuous current through V_{CC} or GND		± 50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DBV package	165	°C/W
		DCK package	259	
		DRY package	340	
		DSF package	300	
		YFP package	123	
		YZP package	123	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V	-3.1	mA
		$V_{CC} = 3$ V	-4	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V	3.1	mA
		$V_{CC} = 3$ V	4	
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		2.3 V to 2.7 V	0.6	1.1		0.6	1.1	V
		3 V to 3.6 V	0.75	1.16		0.75	1.19	
V _{T-} Negative-going input threshold voltage		2.3 V to 2.7 V	0.35	0.6		0.35	0.6	V
		3 V to 3.6 V	0.5	0.85		0.5	0.85	
ΔV _T Hysteresis (V _{T+} – V _{T-})		2.3 V to 2.7 V	0.23	0.6		0.1	0.6	V
		3 V to 3.6 V	0.25	0.56		0.15	0.56	
V _{OH}	I _{OH} = -20 μA	2.3 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
	I _{OH} = -2.3 mA	2.3 V	2.05			1.97		
	I _{OH} = -3.1 mA		1.9			1.85		
	I _{OH} = -2.7 mA	3 V	2.72			2.67		
	I _{OH} = -4 mA		2.6			2.55		
V _{OL}	I _{OL} = 20 μA	2.3 V to 3.6 V		0.1		0.1		V
	I _{OL} = 2.3 mA	2.3 V		0.31		0.33		
	I _{OL} = 3.1 mA			0.44		0.45		
	I _{OL} = 2.7 mA	3 V		0.31		0.33		
	I _{OL} = 4 mA			0.44		0.45		
I _I	All inputs	V _I = 3.6 V or GND	0 V to 3.6 V		0.1		0.5	μA
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V		0.1		0.5	μA
ΔI _{off}		V _I or V _O = 3.6 V	0 V to 0.2 V		0.2		0.5	μA
I _{CC}		V _I = 3.6 V or GND, I _O = 0	2.3 V to 3.6 V		0.5		0.9	μA
ΔI _{CC}	One input at 0.3 V or 1.1 V, Other inputs at 0 or V _{CC} , I _O = 0	2.3 V to 2.7 V				4		μA
	One input at 0.45 V or 1.2 V, Other inputs at 0 or V _{CC} , I _O = 0	3 V to 3.6 V				12		
C _i	V _I = V _{CC} or GND	3.3 V		1.5				pF
C _o	V _O = V _{CC} or GND	3.3 V		3				pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V, V_I = 1.8 V ± 0.15 V (unless otherwise noted)
(see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C _L	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t _{pd}	A, B, or C	Y	5 pF	1.8	2.3	2.9	0.5	6.8	ns
			10 pF	2.3	2.8	3.4	1	7.9	
			15 pF	2.6	3.1	3.8	1	8.7	
			30 pF	3.8	4.4	5.1	1.5	10.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_I = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)
 (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.8	2.3	3.1	0.5	6	ns
			10 pF	2.2	2.8	3.5	1	7.1	
			15 pF	2.6	3.2	5.2	1	7.9	
			30 pF	3.7	4.4	5.2	1.5	10	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_I = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)
 (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	2	2.7	3.5	0.5	5.5	ns
			10 pF	2.4	3.1	3.9	1	6.5	
			15 pF	2.8	3.5	4.3	1	7.4	
			30 pF	4	4.7	5.5	1.5	9.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted)
 (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2	2.5	0.5	8	ns
			10 pF	2	2.4	2.9	1	8.5	
			15 pF	2.3	2.8	3.3	1	9.1	
			30 pF	3.4	3.9	4.4	1.5	9.8	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_I = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)
 (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	1.9	2.4	0.5	5.3	ns
			10 pF	2	2.3	2.7	1	6.1	
			15 pF	2.3	2.7	3.1	1	6.8	
			30 pF	3.4	3.8	4.2	1.5	8.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_I = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)
(see [Figure 12](#))

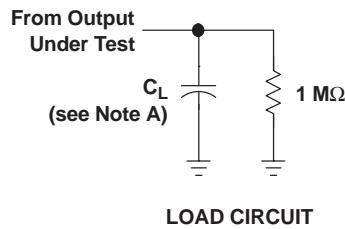
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A, B, or C	Y	5 pF	1.6	2.1	2.7	0.5	4.7	ns
			10 pF	2	2.4	3	1	5.7	
			15 pF	2.3	2.7	3.3	1	6.2	
			30 pF	3.4	3.8	4.4	1.5	7.8	

OPERATING CHARACTERISTICS

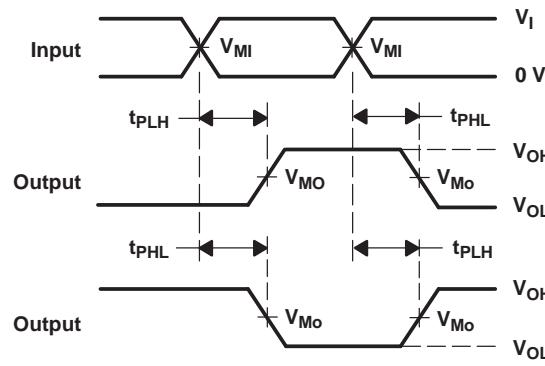
 $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
		TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	4	5	pF

PARAMETER MEASUREMENT INFORMATION



	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	$V_I/2$	$V_I/2$
V_{MO}	$V_{CC}/2$	$V_{CC}/2$



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, slew rate $\geq 1 \text{ V/ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 12. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision H (May 2010) to Revision I	Page
• Updated FUNCTION SELECTION Table.	2
• Updated figure caption.	5
• Updated figure caption.	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1T98DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R	Samples
SN74AUP1T98DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT6R	Samples
SN74AUP1T98DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR	Samples
SN74AUP1T98DCKT	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR	Samples
SN74AUP1T98DCKTG4	ACTIVE	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TKR	Samples
SN74AUP1T98DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK	Samples
SN74AUP1T98DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	TK	Samples
SN74AUP1T98YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TK2 ~ TKN)	Samples
SN74AUP1T98YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TK7 ~ TKN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

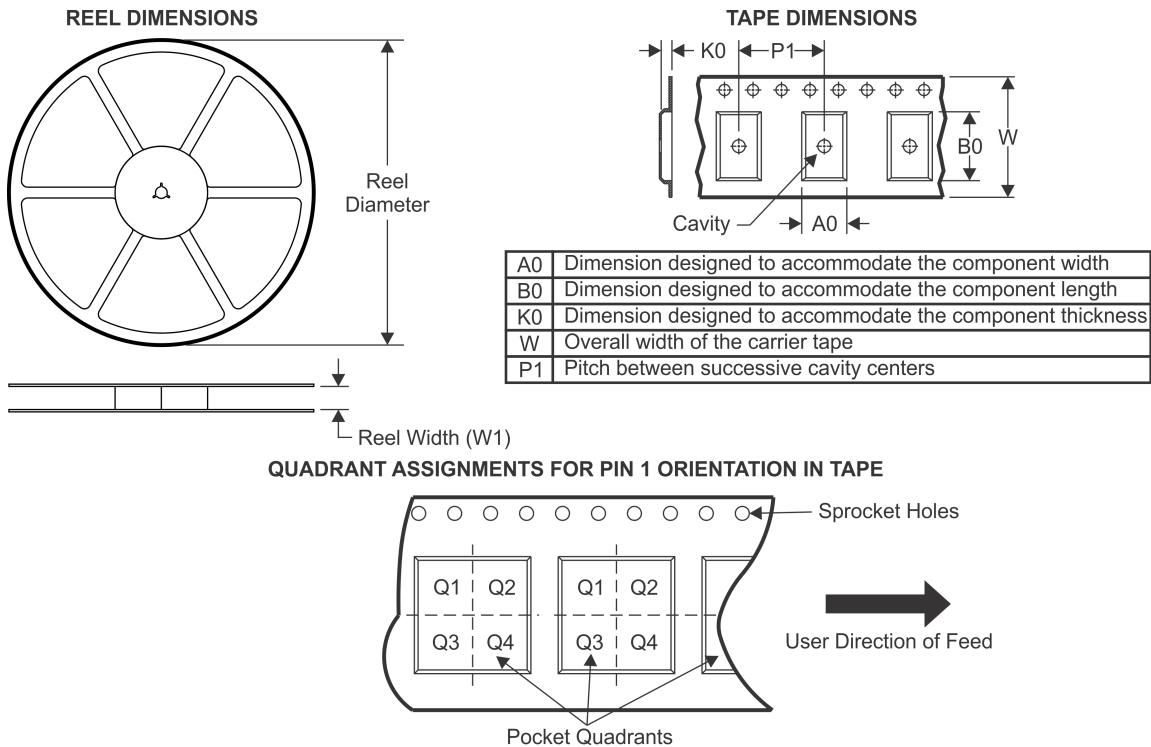
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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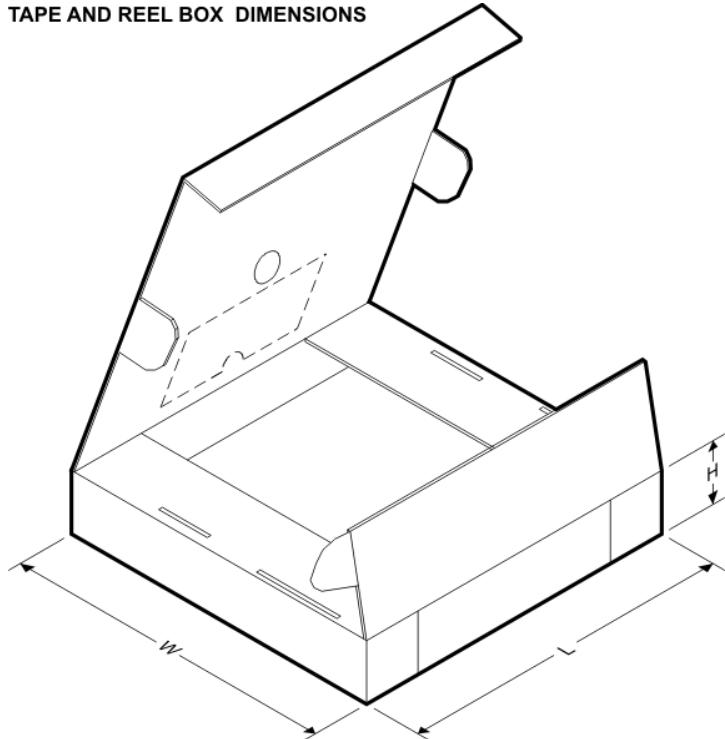
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1T98DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T98DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1T98DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T98DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1T98DRYR	SON	DRY	6	5000	180.0	8.4	1.25	1.6	0.7	4.0	8.0	Q1
SN74AUP1T98DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1T98YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1T98YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



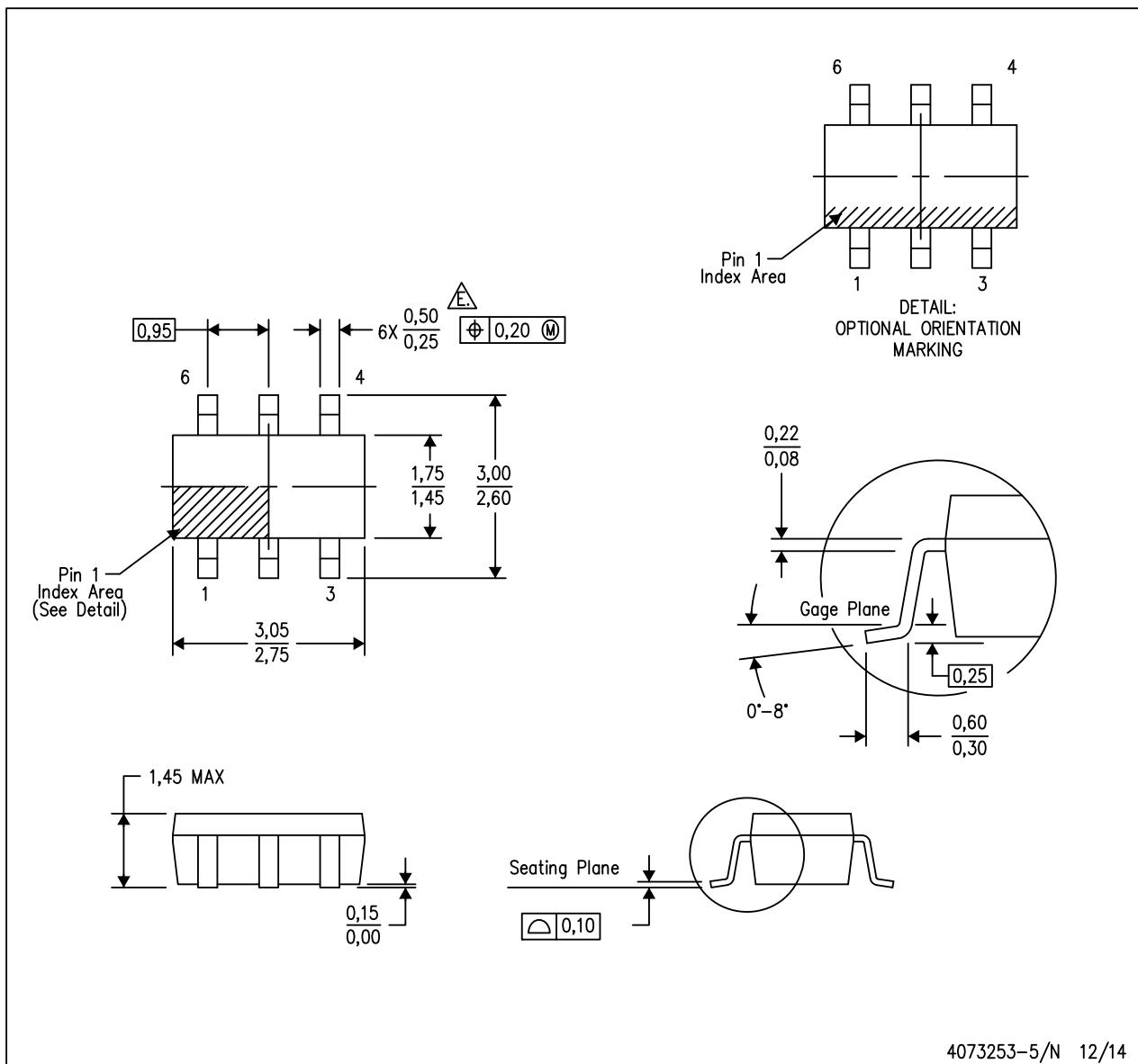
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1T98DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1T98DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1T98DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74AUP1T98DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1T98DRYR	SON	DRY	6	5000	202.0	201.0	28.0
SN74AUP1T98DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1T98YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1T98YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-5/N 12/14

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.

Falls within JEDEC MO-178 Variation AB, except minimum lead width.

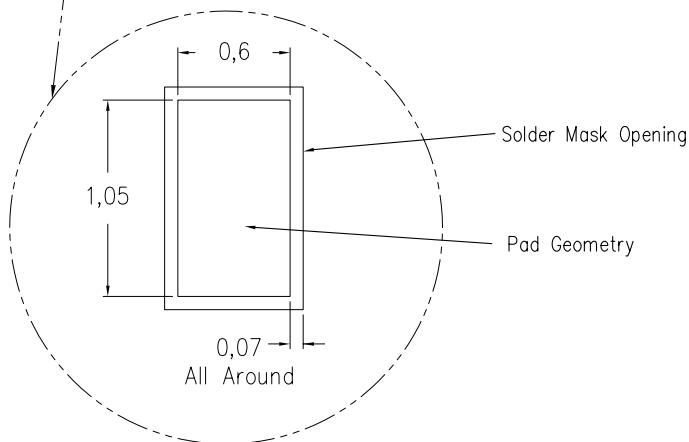
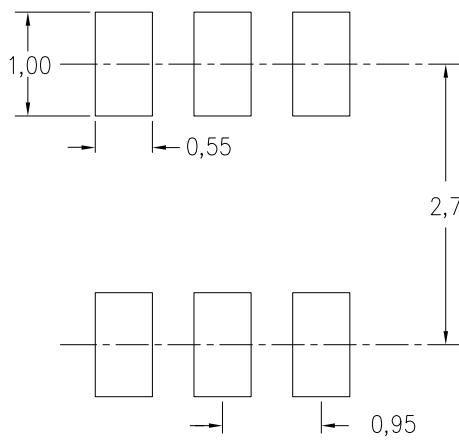
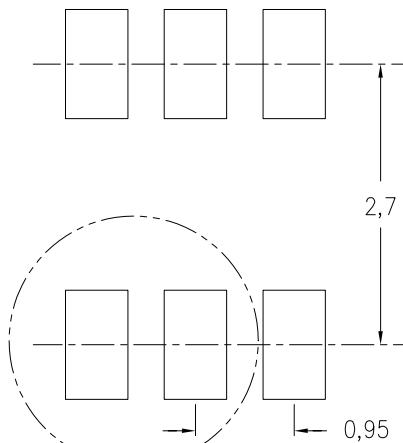
LAND PATTERN DATA

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4209593-4/C 08/11

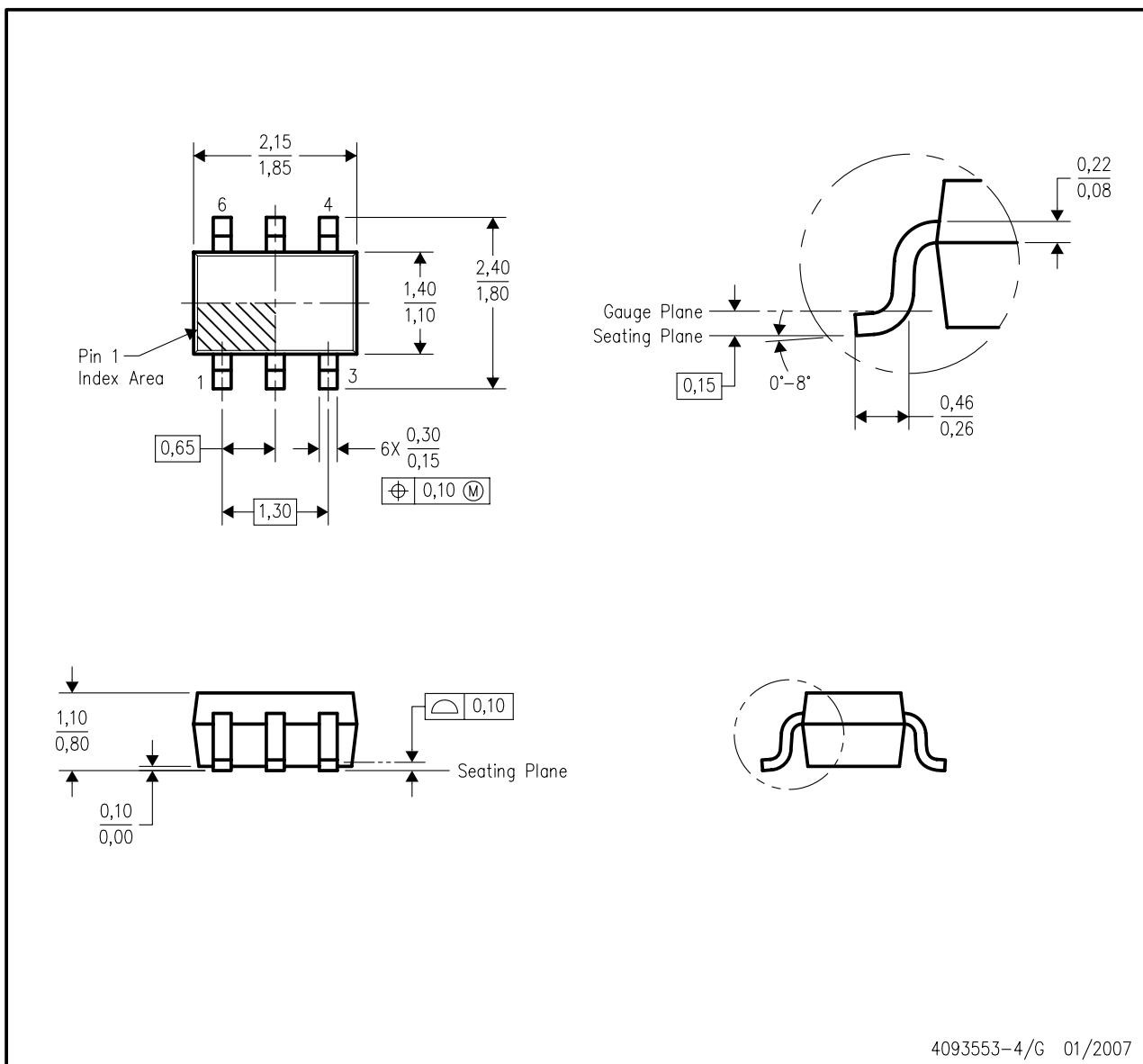
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

MECHANICAL DATA

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



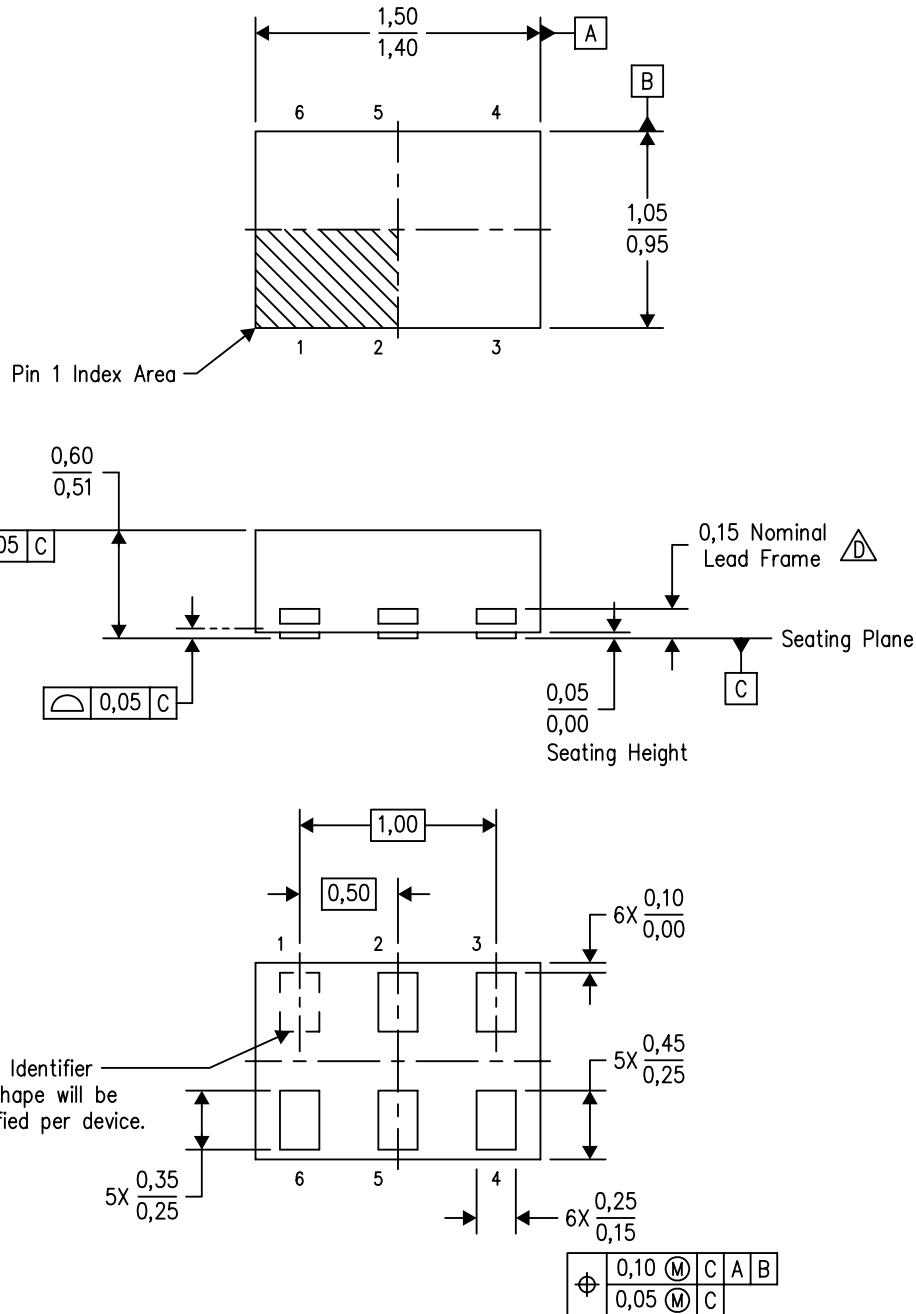
4093553-4/G 01/2007

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AB.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



Bottom View

4207181/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. SON (Small Outline No-Lead) package configuration.

D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

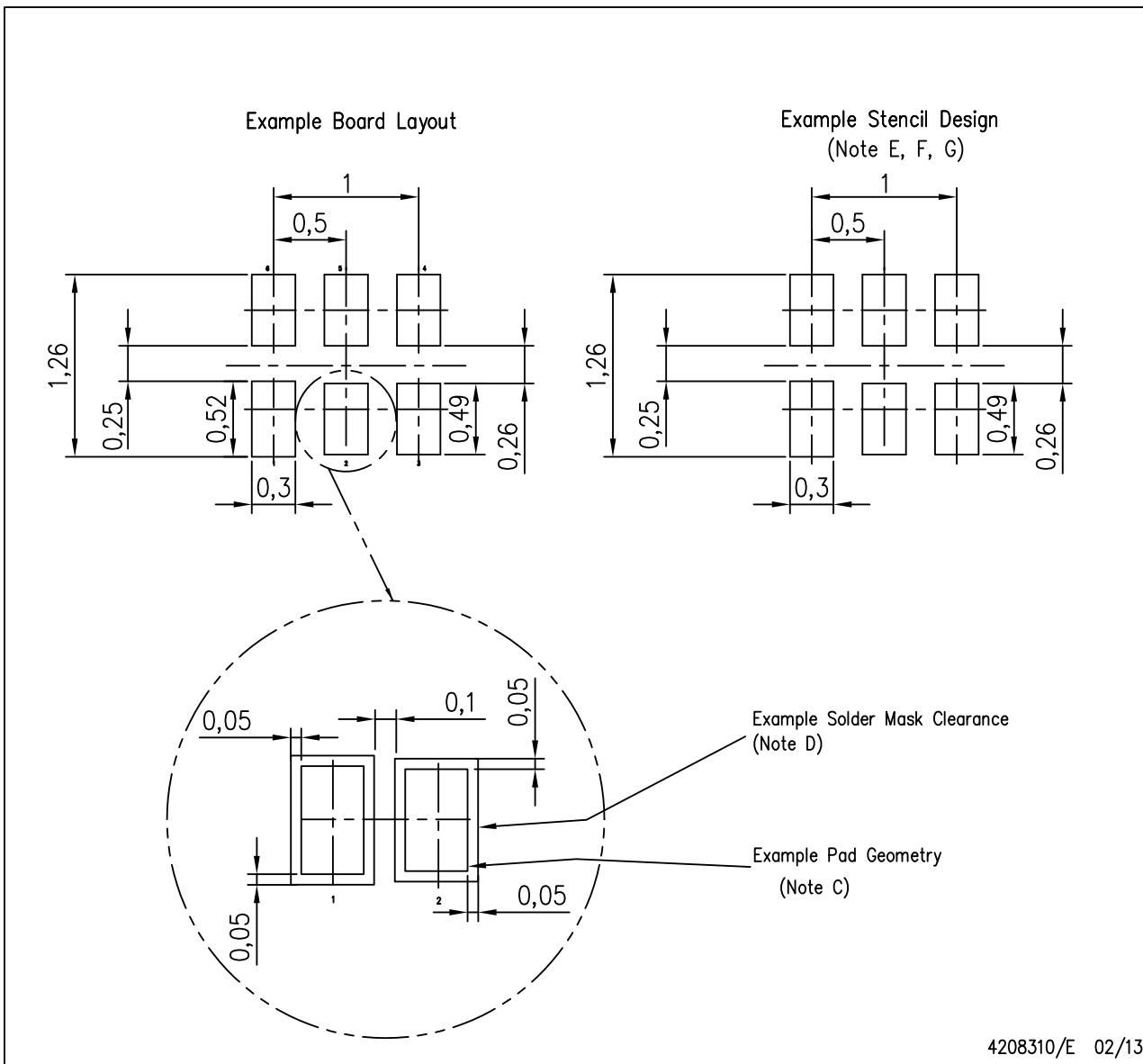
E. This package complies to JEDEC MO-287 variation UFAD.

F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

LAND PATTERN DATA

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4208310/E 02/13

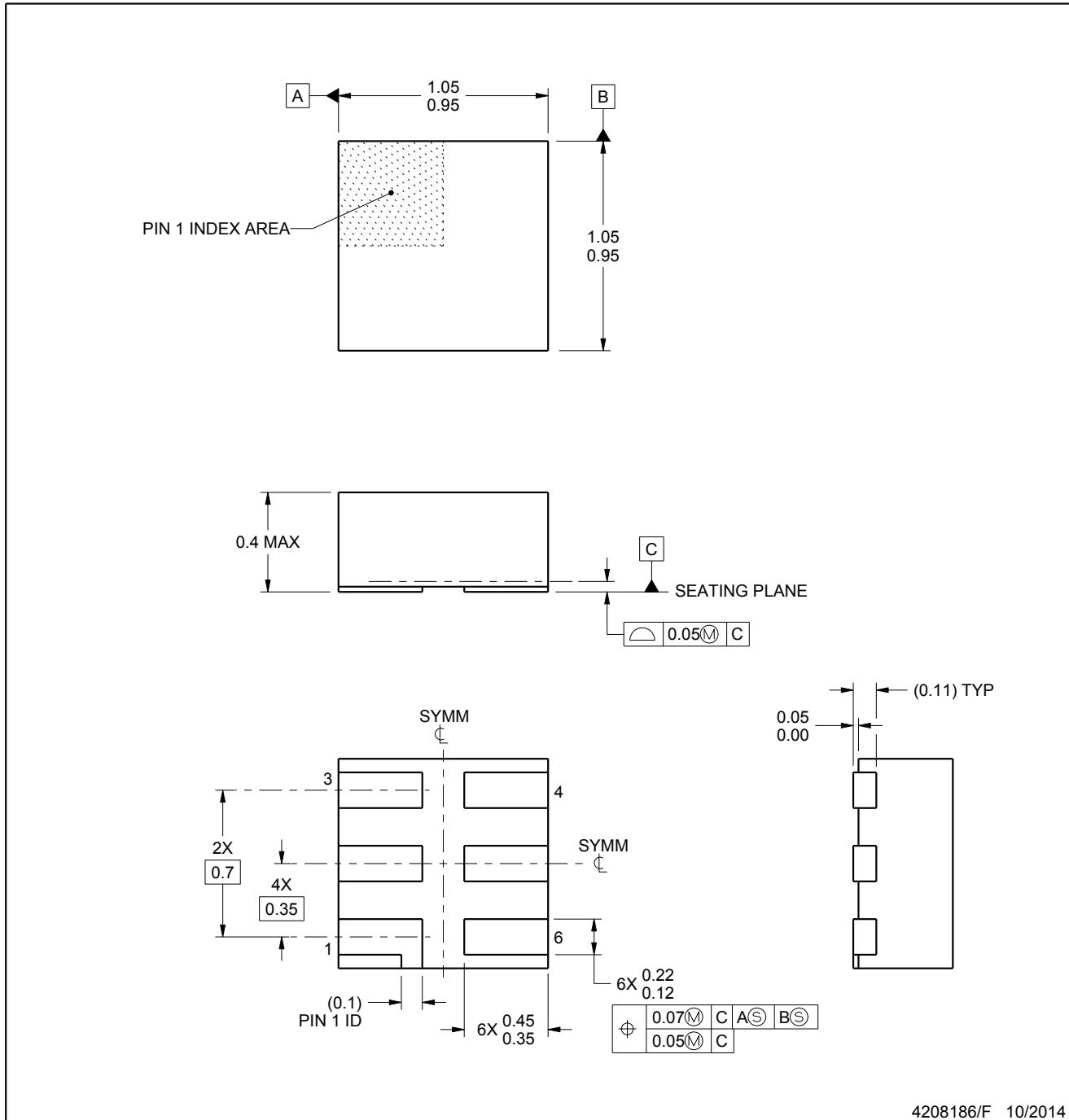
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66 . Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

MECHANICAL DATA

DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4208186/F 10/2014

NOTES:

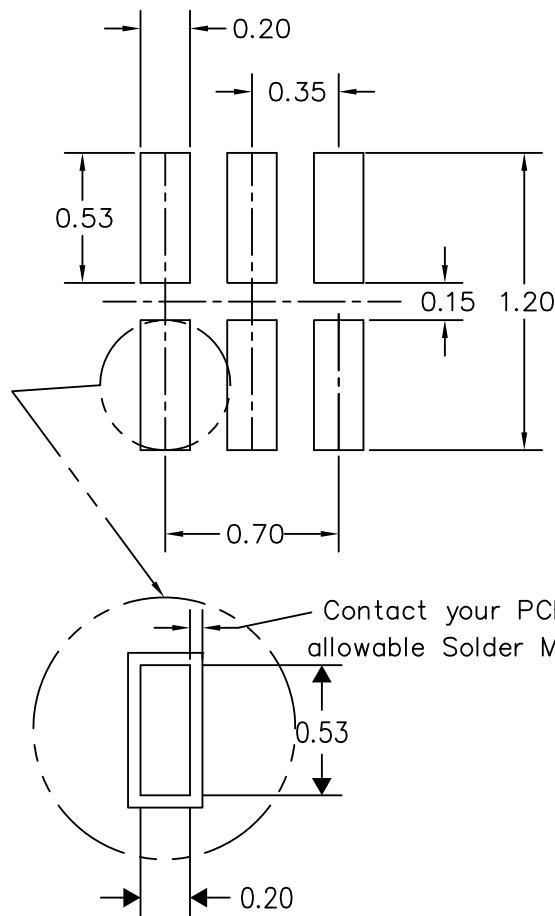
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

LAND PATTERN DATA

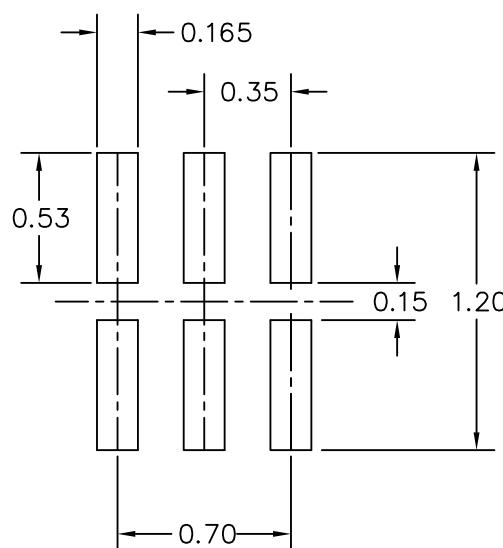
DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern



Stencil Pattern



4210277/D 05/12

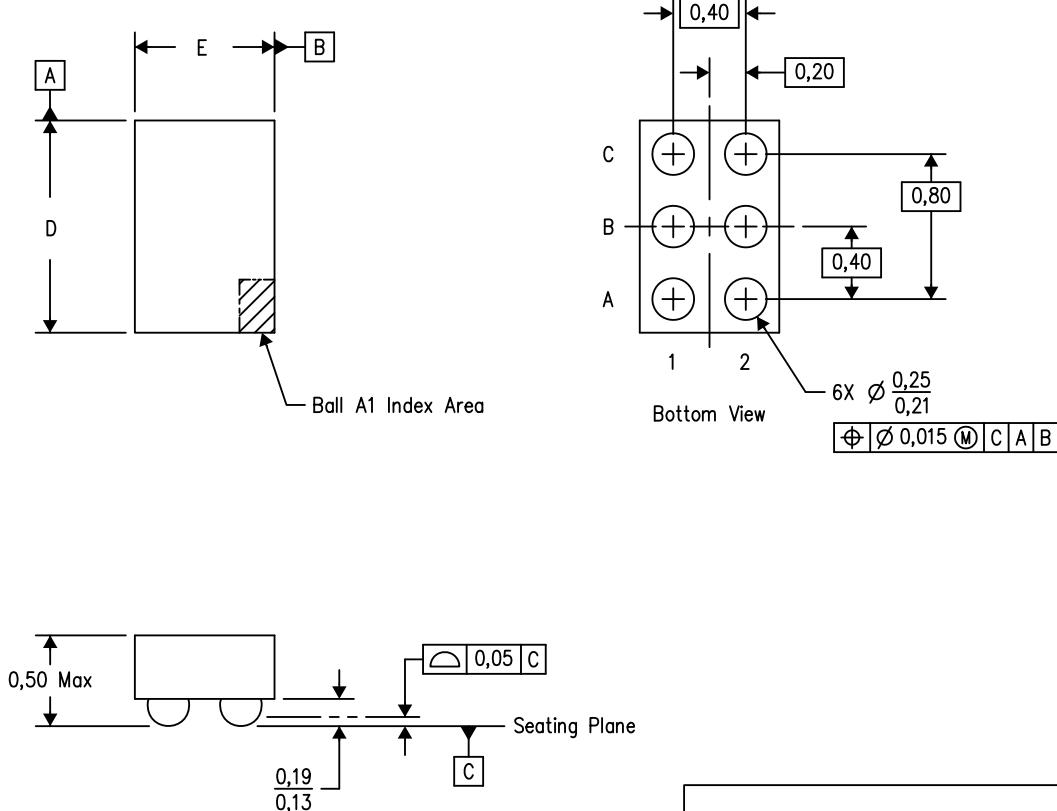
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- Component placement force should be minimized to prevent excessive paste block deformation.

MECHANICAL DATA

YFP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



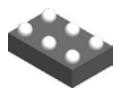
4206986-3/T 05/13

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

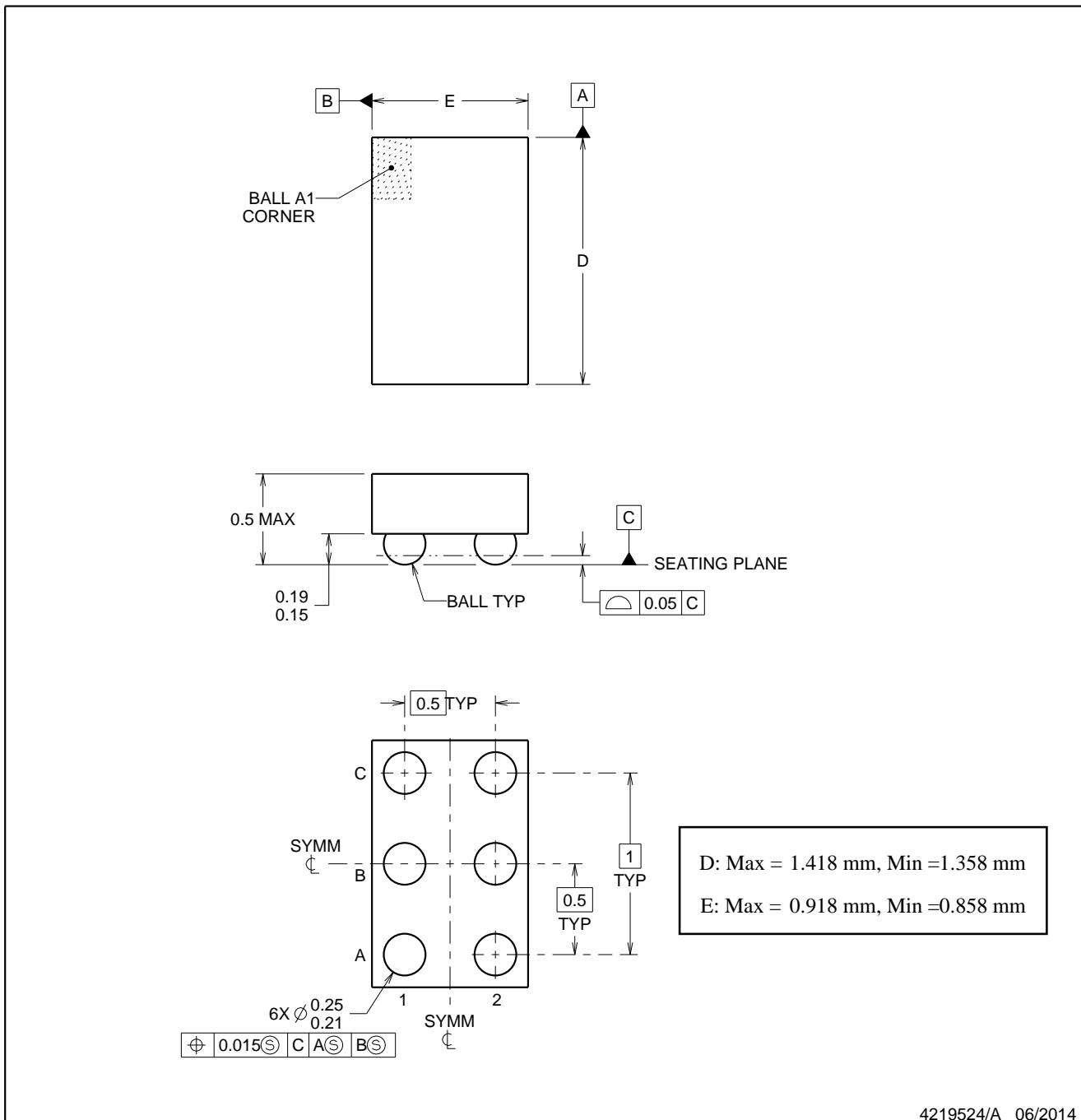
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

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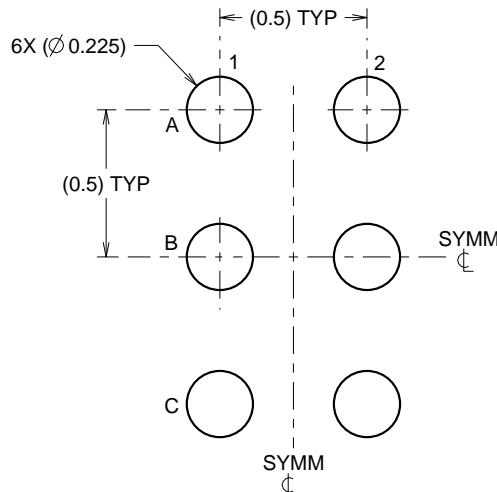
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

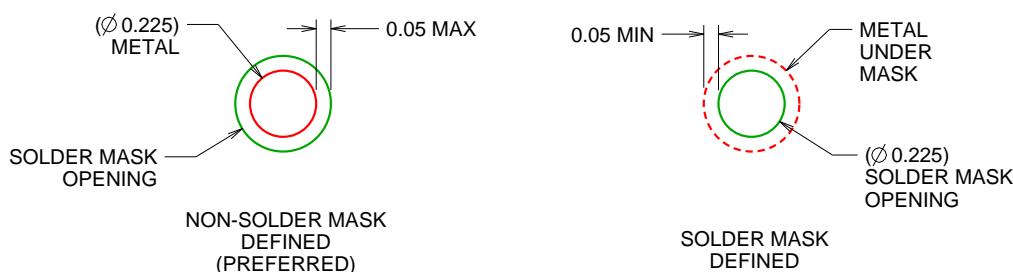
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

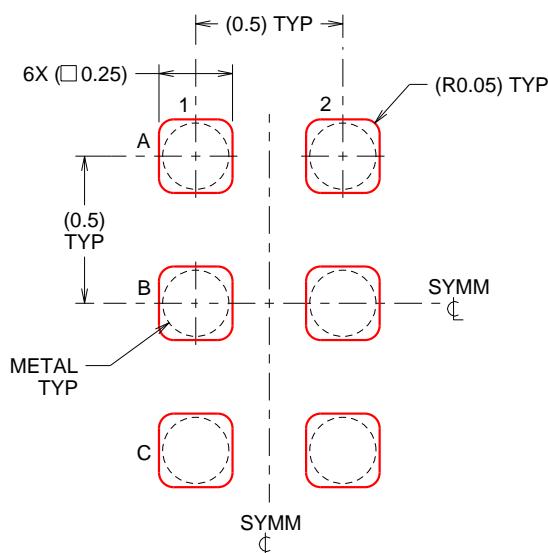
4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN**YZP0006****DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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