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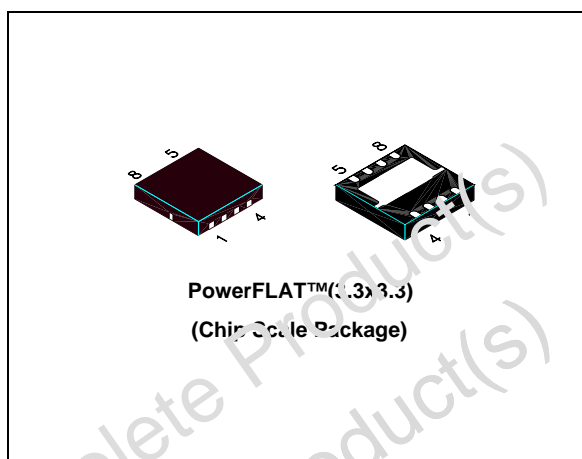
# STL8NH3LL

N-channel 30 V, 0.012 Ω, 8 A - PowerFLAT™ (3.3x3.3)  
 ultra low gate charge STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL8NH3LL	30V	<0.015Ω	8A <sup>(1)</sup>

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device
- In compliance with the 2002/95/EC European directive



## Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique STripFET™ technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

## Applications

- Switching application

Figure 1. Internal schematic diagram

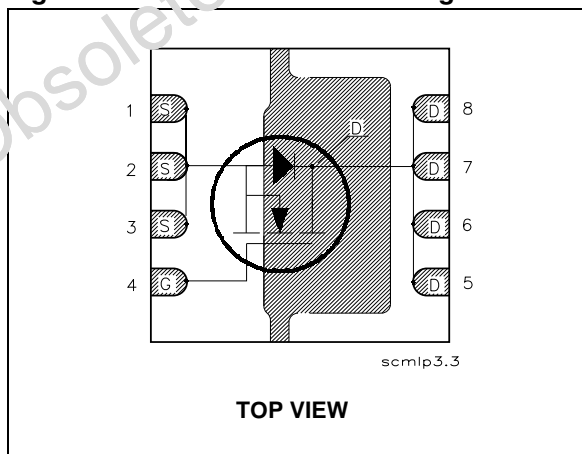


Table 1. Device summary

Order code	Marking	Package	Packaging
STL8NH3LL	8NH3L	PowerFLAT™ (3.3x3.3)	Tape and reel

## Contents

1	<b>Electrical ratings</b> .....	3
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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 18$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	8	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	32	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	?	W
	Derating factor	0.4	W/ $^\circ\text{C}$
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. The value is rated according  $R_{thj-pcb}$
2. Pulse width limited by safe operating area.
3. The vaule is rated according  $R_{thj-c}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec
2. Steady state

Electrical characteristics

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## 2 Electrical characteristics

(T<sub>CASE</sub>= 25 °C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-Source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = max rating, V <sub>DS</sub> = max rating @ 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±18 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		2.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4 A		0.012 0.0135	0.015 0.017	Ω Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> =15 V, I <sub>D</sub> = 4 A		30		S
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =25 V, f=1 MHz, V <sub>GS</sub> =0		965		pF
C <sub>oss</sub>	Output capacitance			285		pF
C <sub>rss</sub>	Reverse transfer capacitance			38		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> =15 V, I <sub>D</sub> = 8 A		9	12	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> =4.5 V		3.7		nC
Q <sub>gd</sub>	Gate-drain charge	(see Figure 8)		3		nC
R <sub>G</sub>	Gate input resistance	f=1 MHz gate DC bias = 0 test signal level = 20mV open drain	0.5	1.5	2.5	Ω

1. Pulsed: pulse duration= 300 μs, duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> =15 V, I <sub>D</sub> = 4 A, R <sub>G</sub> =4.7 Ω, V <sub>GS</sub> =4.5 V (see Figure 14)		15		ns	
t <sub>r</sub>	Rise time		-	32	-	ns	
t <sub>d(off)</sub>	Turn-off delay time				18		ns
t <sub>f</sub>	Fall Time				8.5		ns

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**Electrical characteristics**

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=8\text{ A}, V_{GS}=0$	-		1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=8\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD}=20\text{ V}, T_j=150\text{ }^\circ\text{C}$ (see Figure 16)	-	24 17.4 1.45		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300  $\mu\text{s}$ , duty cycle 1.5 %

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Electrical characteristics

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance

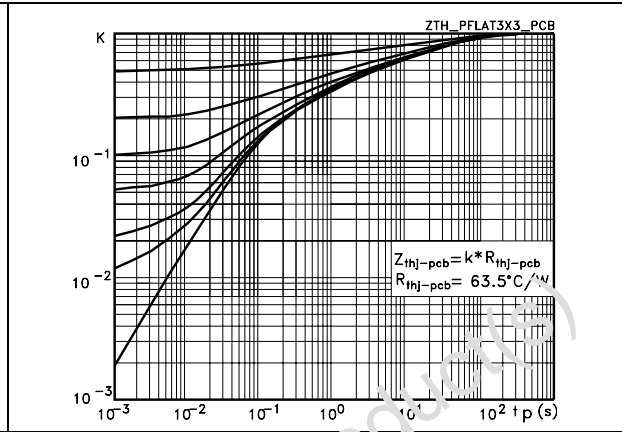
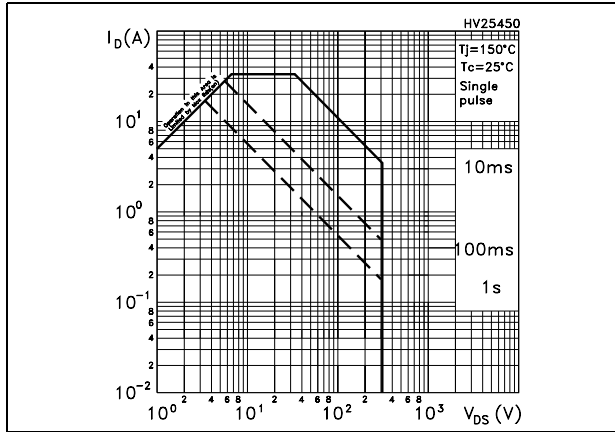


Figure 4. Output characteristics

Figure 5. Transfer characteristics

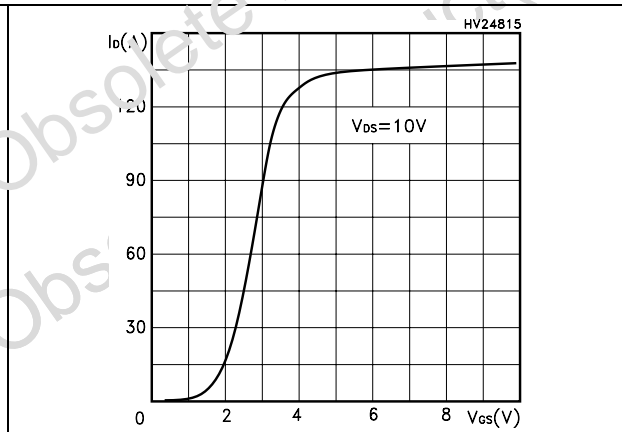
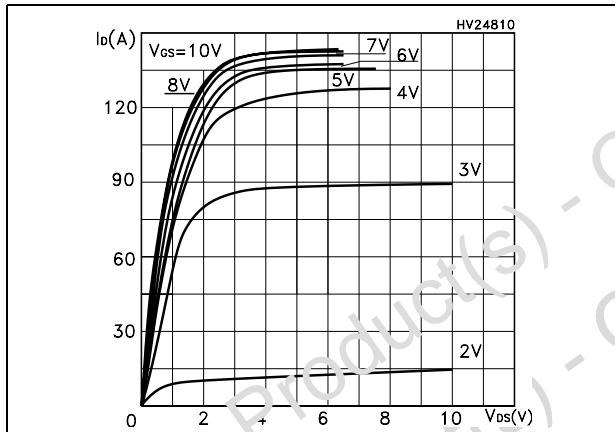
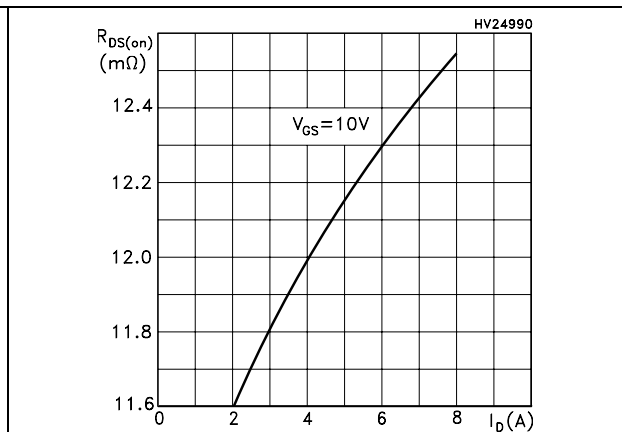
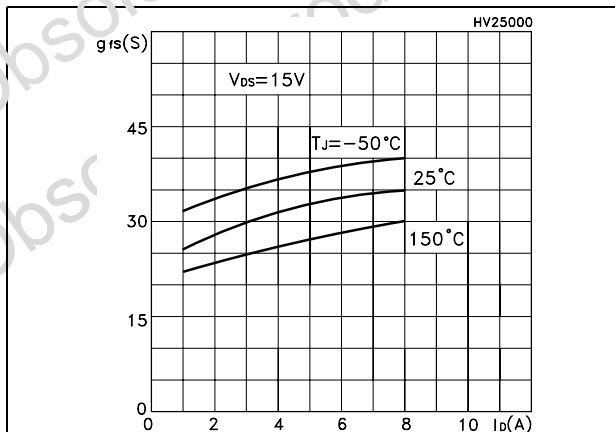


Figure 6. Transconductance

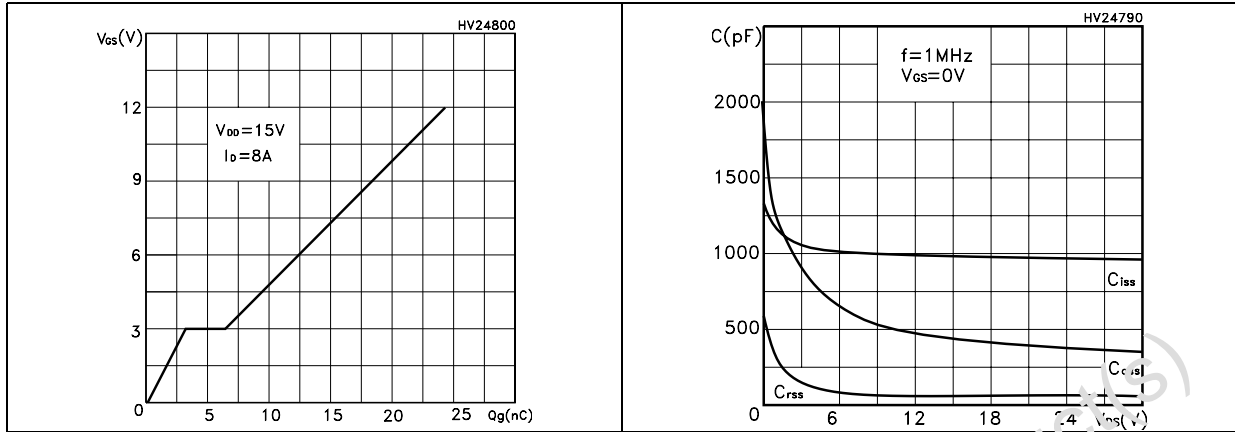
Figure 7. Static drain-source on resistance



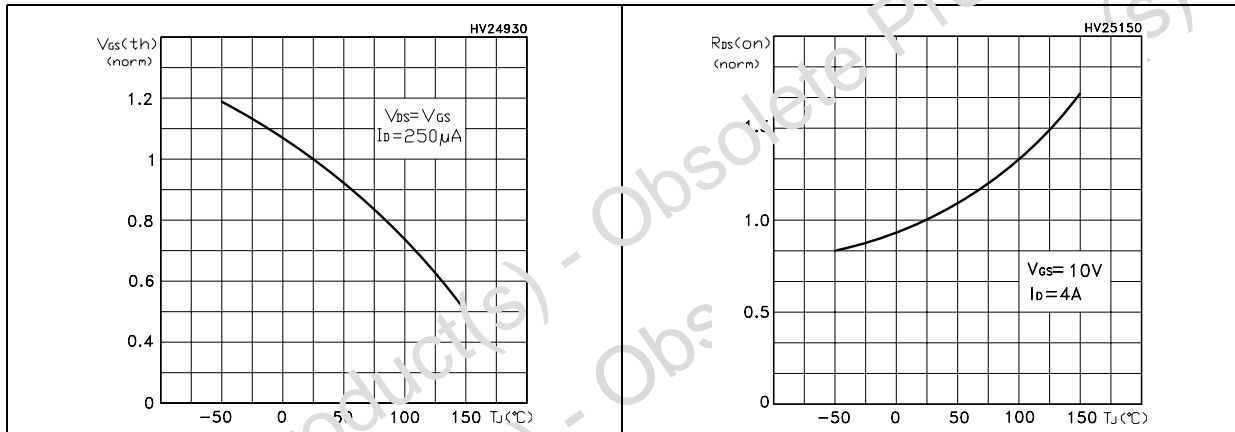
**STL8NH3LL**

**Electrical characteristics**

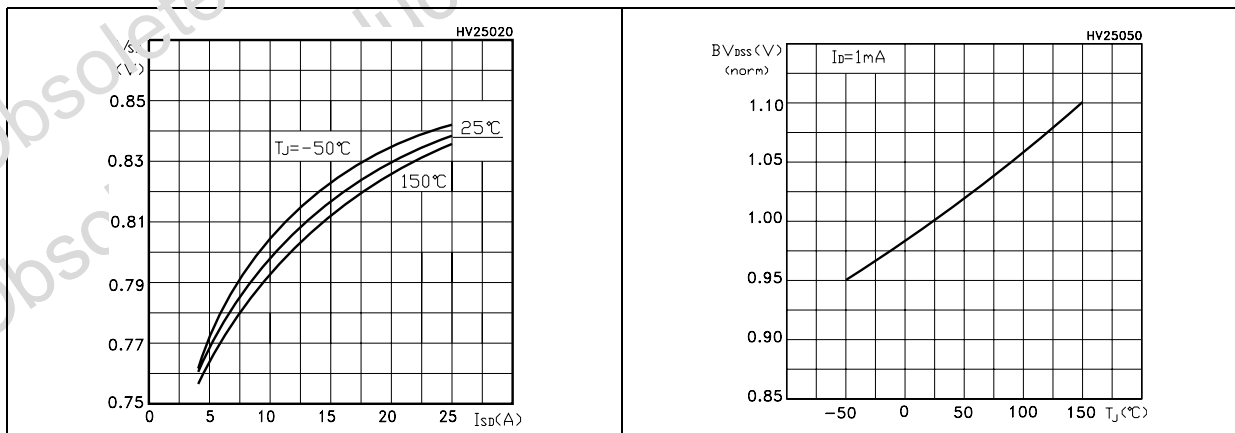
**Figure 8. Gate charge vs gate-source voltage** **Figure 9. Capacitance variations**



**Figure 10. Normalized gate threshold voltage vs temperature** **Figure 11. Normalized on resistance vs temperature**



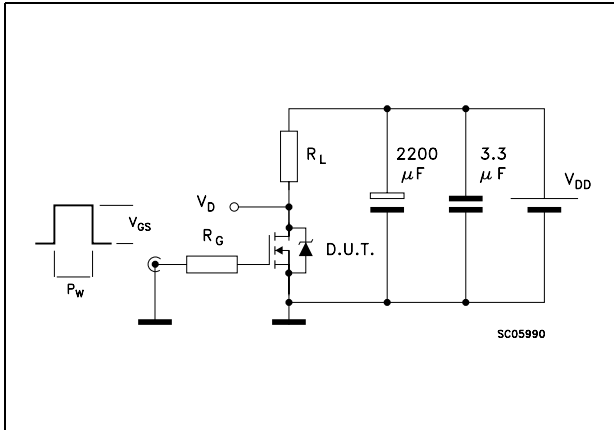
**Figure 12. Source-drain diode forward characteristics** **Figure 13. Normalized  $B_{V_{DS}}$  vs temperature**



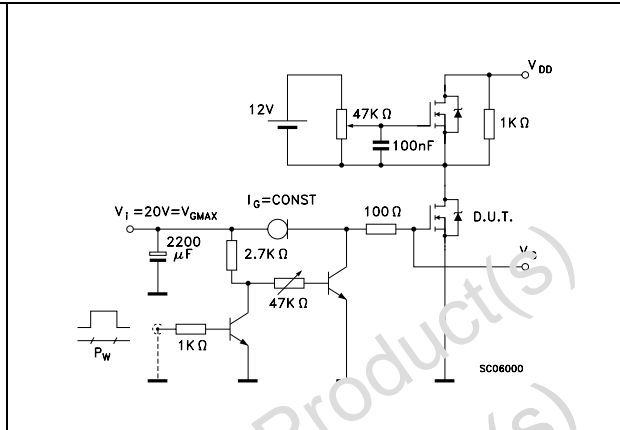


### 3 Test circuits

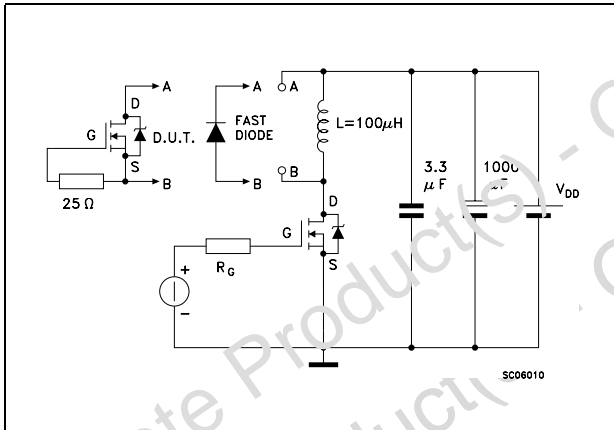
**Figure 14. Switching times test circuit for resistive load**



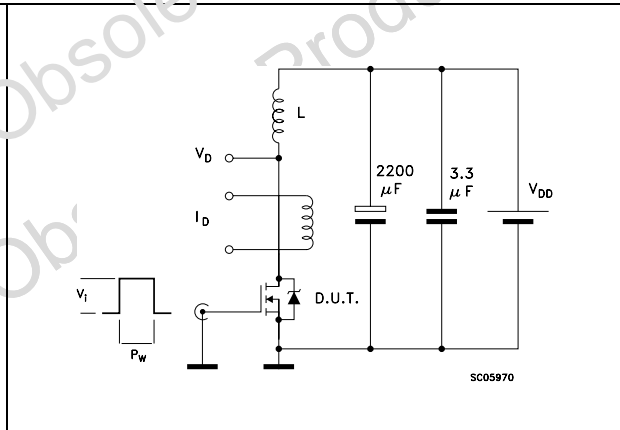
**Figure 15. Gate charge test circuit**



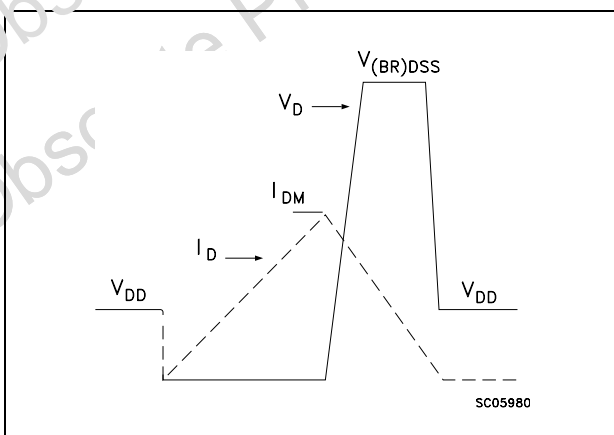
**Figure 16. Inductive load switching and diode recovery times**



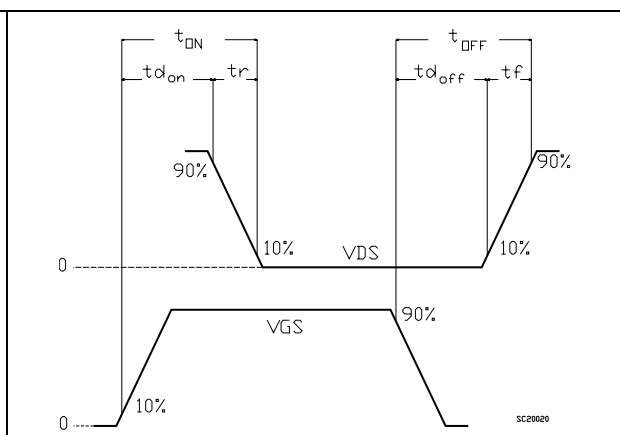
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**



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Package mechanical data

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

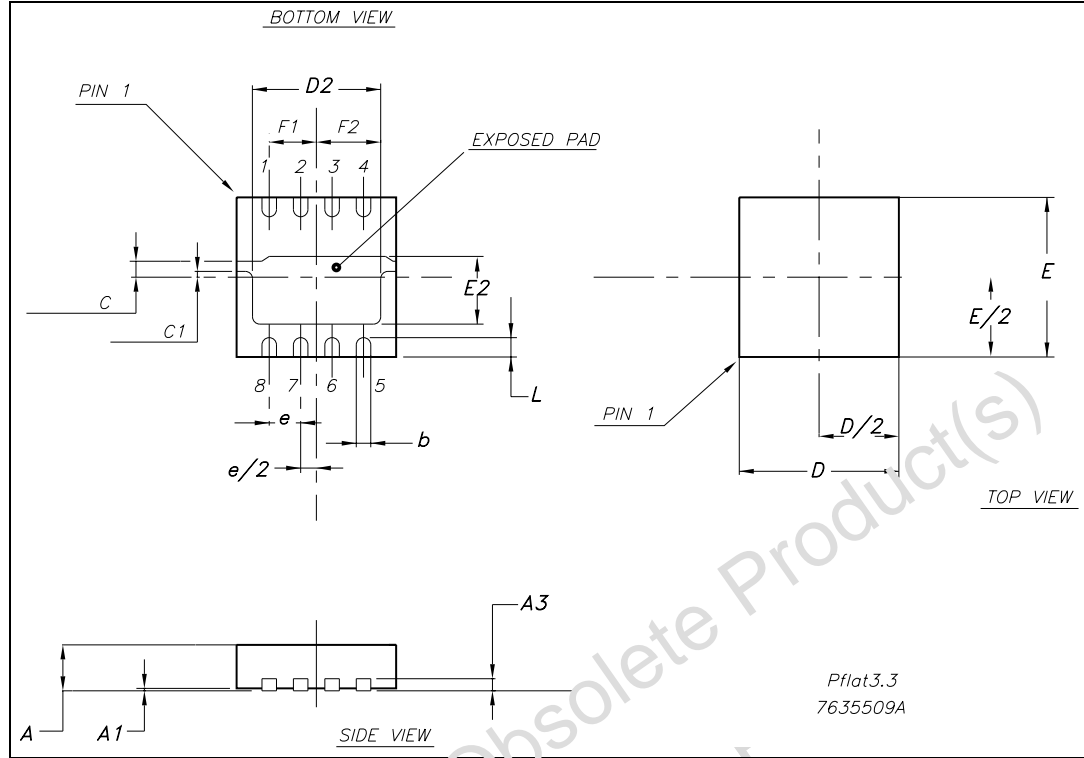
**Table 8. Package dimensions**

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.23	0.30	0.38	0.009	0.011	0.015
C		0.328			0.012	
C1		0.12			0.004	
D		3.30			0.13	
D2	2.50	2.65	2.75	0.098	0.104	0.108
E		3.30			0.13	
E2	1.25	1.40	1.50	0.049	0.055	0.059
F		1.325			0.052	
F1		0.975			0.038	
e		0.65			0.025	
L	0.30		0.50	0.011		0.019

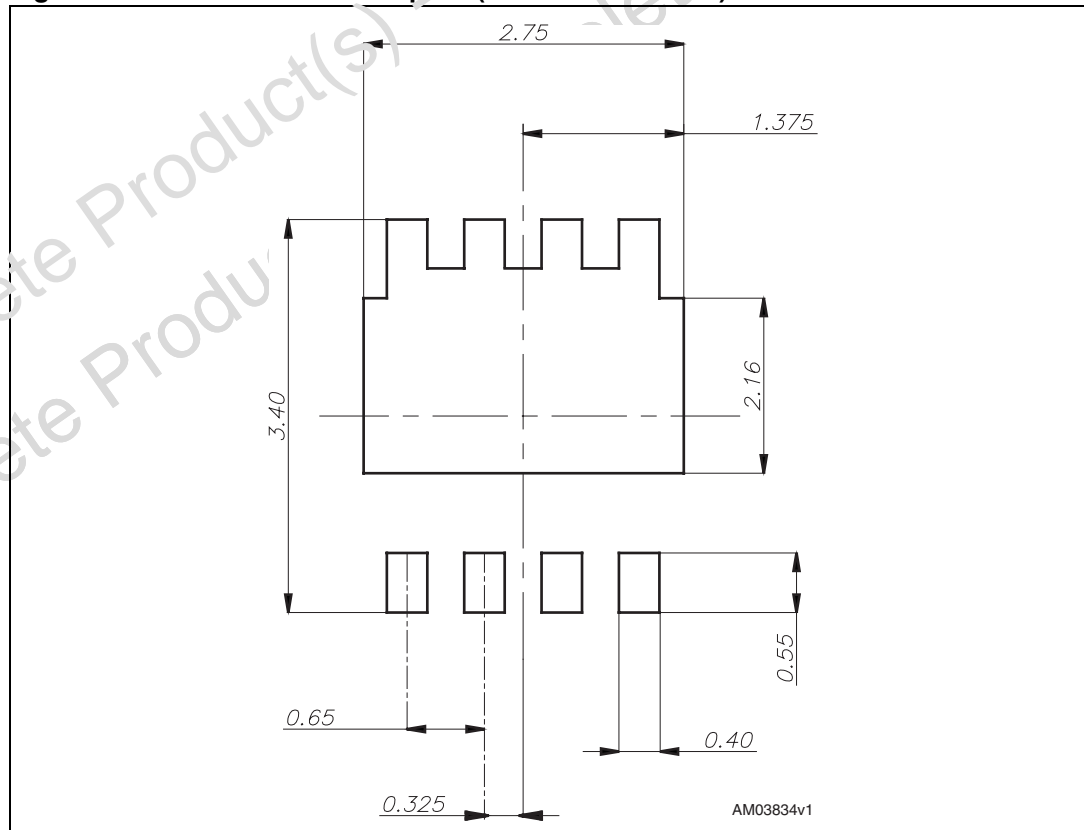
**Package mechanical data**

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**Figure 20. Package drawing**



**Figure 21. Recommended footprint (dimensions in mm)**



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
21-Jul-2004	1	First release
05-Oct-2004	2	Values changed
19-Oct-2004	3	New value inserted
22-Nov-2004	4	Document updated
21-Feb-2005	5	Final version
18-Apr-2005	6	Modified <a href="#">Figure 4</a> , <a href="#">Figure 6.</a> , <a href="#">Figure 9.</a> , <a href="#">Figure 10.</a>
14-Mar-2006	7	New template
10-Sep-2009	8	Inserted <a href="#">Figure 21</a>

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