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[IRFPS29N60LPBF](#)

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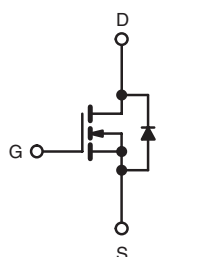
IRFPS29N60L, SiHFPS29N60L

Vishay Siliconix

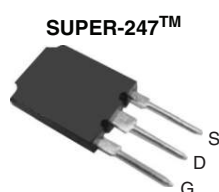
Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.175
Q_g (Max.) (nC)	220	
Q_{gs} (nC)	67	
Q_{gd} (nC)	96	
Configuration	Single	



N-Channel MOSFET



FEATURES

- Super Fast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhances dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offer Improved Noise Immunity
- Lead (Pb)-free Available



RoHS*
COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION

Package	SUPER-247™
Lead (Pb)-free	IRFPS29N60LPbF SiHFPS29N60L-E3
SnPb	IRFPS29N60L SiHFPS29N60L

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	600	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	29	A
		T _C = 100 °C		18	
Pulsed Drain Current ^a			I _{DM}	110	
Linear Derating Factor				3.8	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	570	mJ
Repetitive Avalanche Current ^a			I _{AR}	29	A
Repetitive Avalanche Energy ^a			E _{AR}	48	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	480	W
Peak Diode Recovery dV/dt ^c			dV/dt	15	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.5\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 29\text{ A}$ (see fig.12a).
- $I_{SD} \leq 29\text{ A}$, $dI/dt \leq 830\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

IRFPS29N60L, SiHFPS29N60L

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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient ^a	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain) ^a	R_{thJC}	-	0.26	

Note

a. R_{th} is measured at T_J approximately 90 °C.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.53	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	2.0	mA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 17 A ^b	-	0.175	0.21	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 17 A ^b		15	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^b		-	6160	-	pF
Output Capacitance	C _{oss}			-	530	-	
Reverse Transfer Capacitance	C _{rss}			-	44	-	
Effective Output Capacitance	C _{oss} eff.	V _{DS} = 0 V to 480 V ^c		-	250	-	pF
Effective Output Capacitance (Energy Related)	C _{oss} eff. (ER)			-	190	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 29 A, V _{DS} = 480 V, see fig. 7 and 15 ^b	-	-	220	nC
Gate-Source Charge	Q _{gs}			-	-	67	
Gate-Drain Charge	Q _{gd}			-	-	96	
Internal Gate Resistance	R _G	f = 1 MHz, open drain		-	0.86	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} =300 V, I _D = 29 A, R _G = 4.3 Ω, V _{GS} = 10 V, see fig. 11a and 11b ^b		-	34	-	ns
Rise Time	t _r			-	100	-	
Turn-Off Delay Time	t _{d(off)}			-	66	-	
Fall Time	t _f			-	54	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	29	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	110	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 29 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 29 A T _J = 125 °C, dI/dt = 100 A/μs ^b		-	130	190	ns
				-	240	360	
Body Diode Reverse Recovery Charge	Q _{rr}			-	630	950	μC
				-	1820	2720	
Body Diode Recovery Current	I _{RRM}	T _J = 25 °C		-	9.4	14	A
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

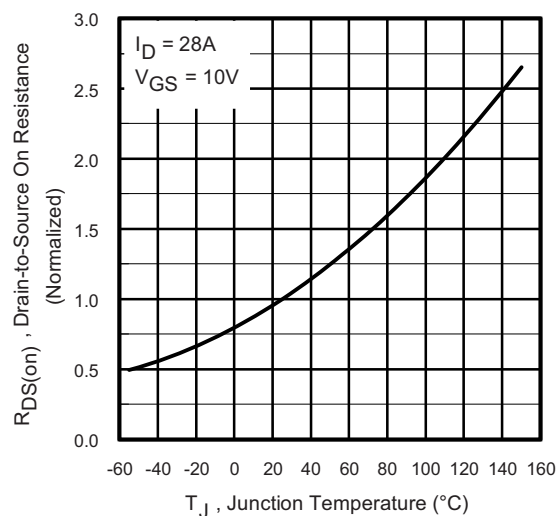
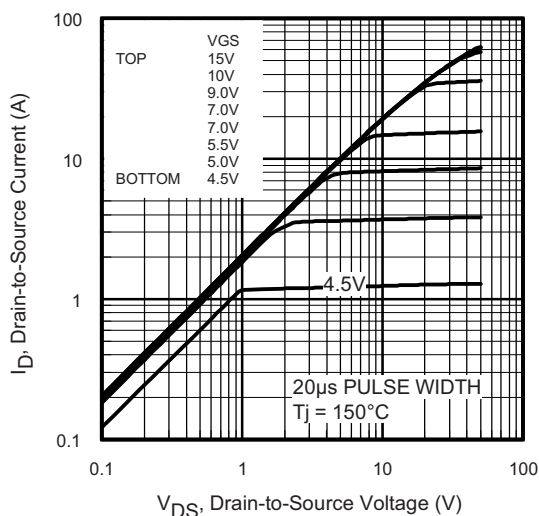
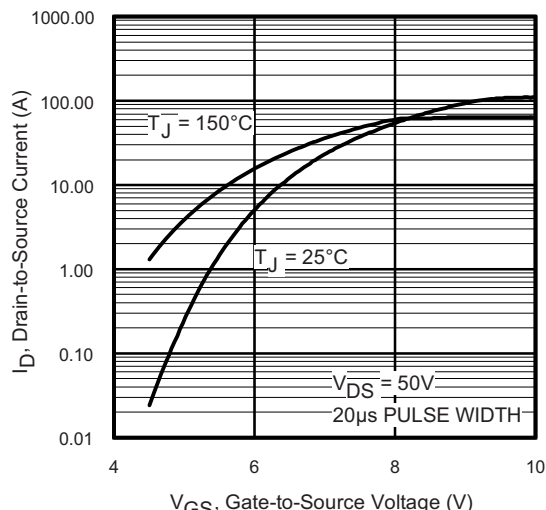
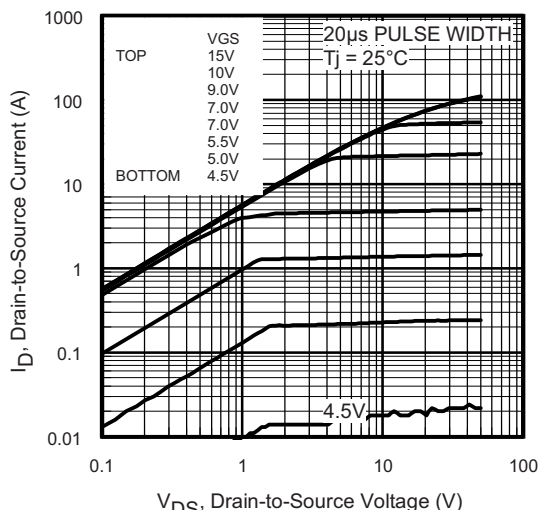
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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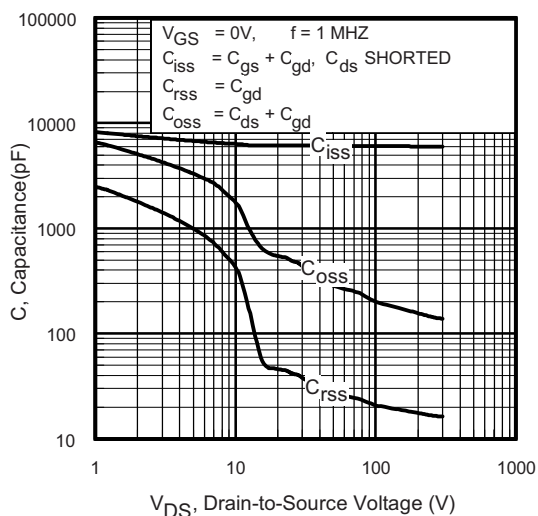


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

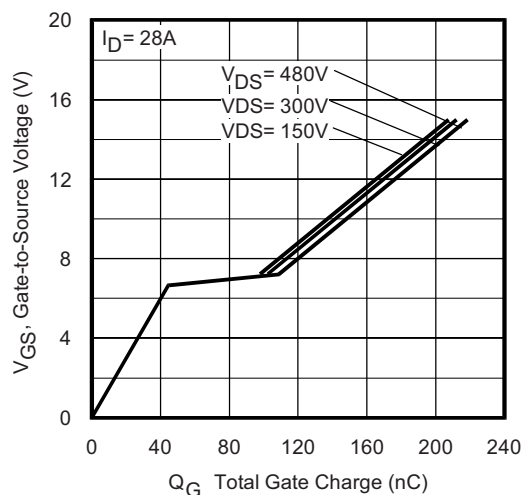


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

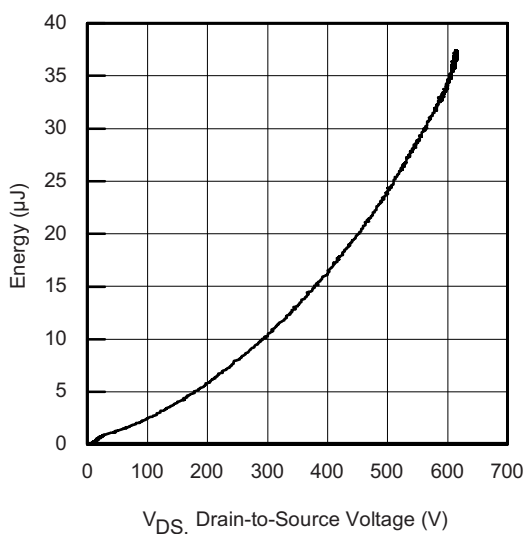


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

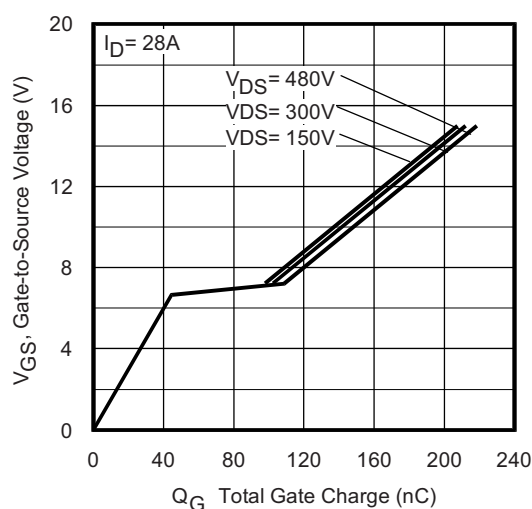


Fig. 8 - Typical Source-Drain Diode Forward Voltage



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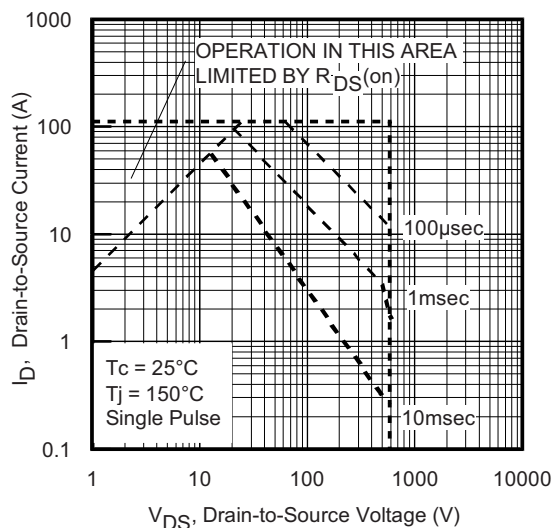


Fig. 9 - Maximum Safe Operating Area

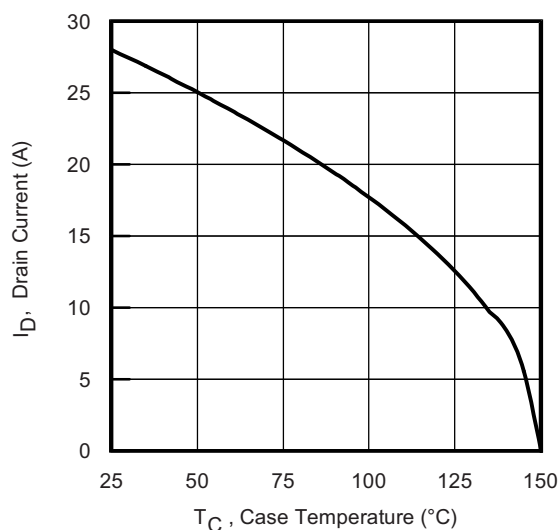


Fig. 10 - Maximum Drain Current vs. Case Temperature

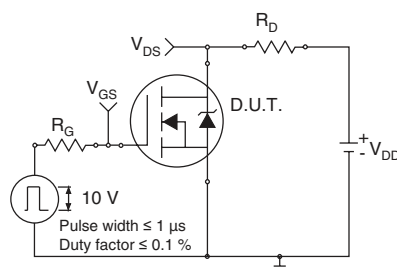


Fig. 11a - Switching Time Test Circuit

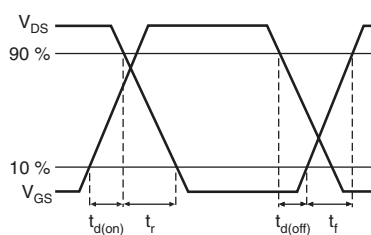


Fig. 11b - Switching Time Waveforms

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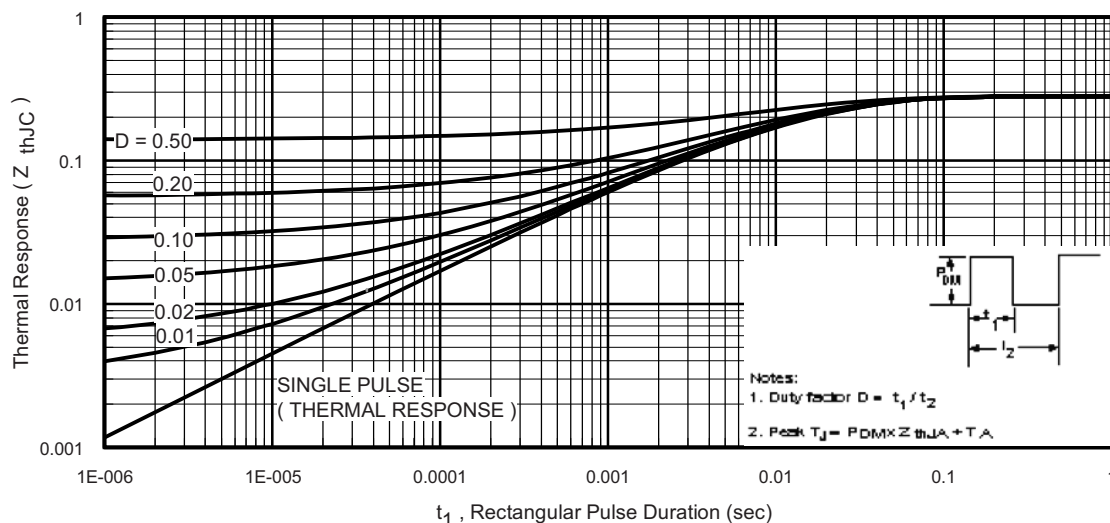


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

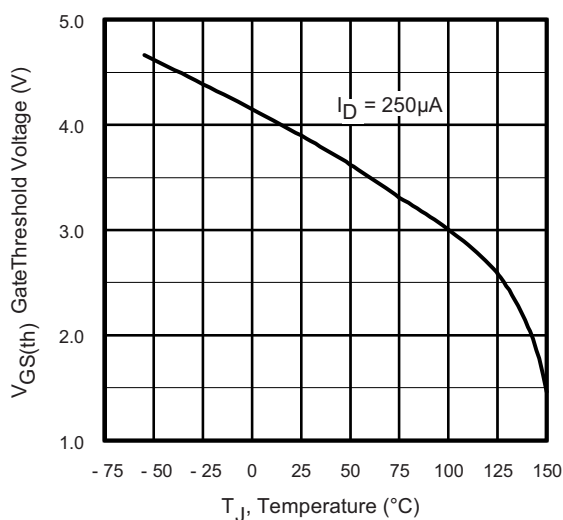


Fig. 13 - Threshold Voltage vs. Temperature

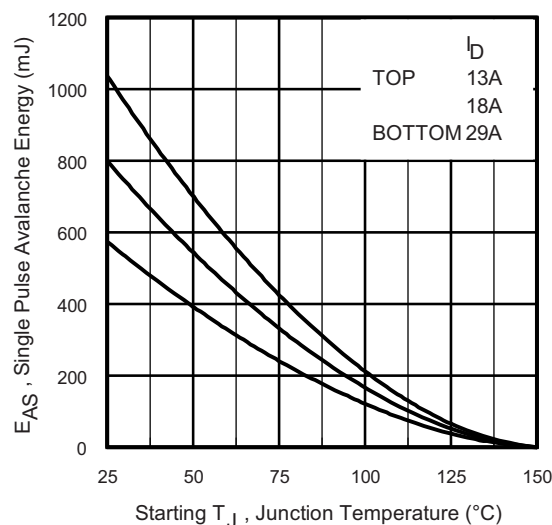


Fig. 14a - Maximum Avalanche Energy vs. Drain Current

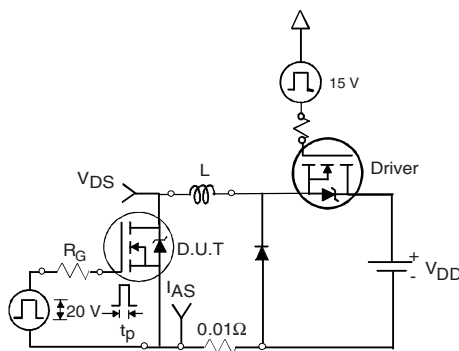


Fig. 14b - Unclamped Inductive Test Circuit



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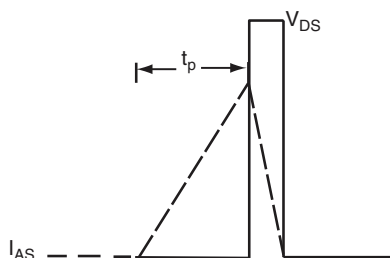


Fig. 14c - Unclamped Inductive Waveforms

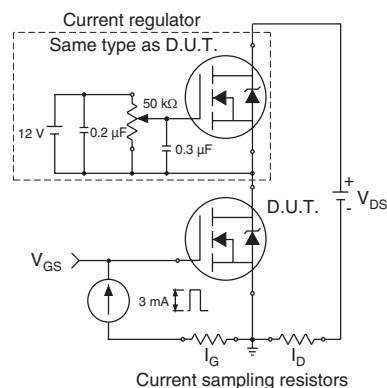


Fig. 15a - Gate Charge Test Circuit

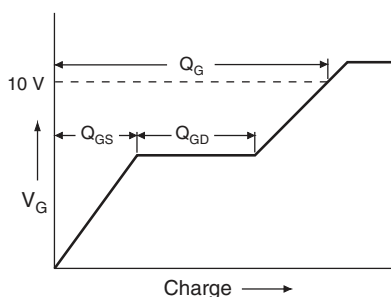


Fig. 15b - Basic Gate Charge Waveform

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Peak Diode Recovery dV/dt Test Circuit

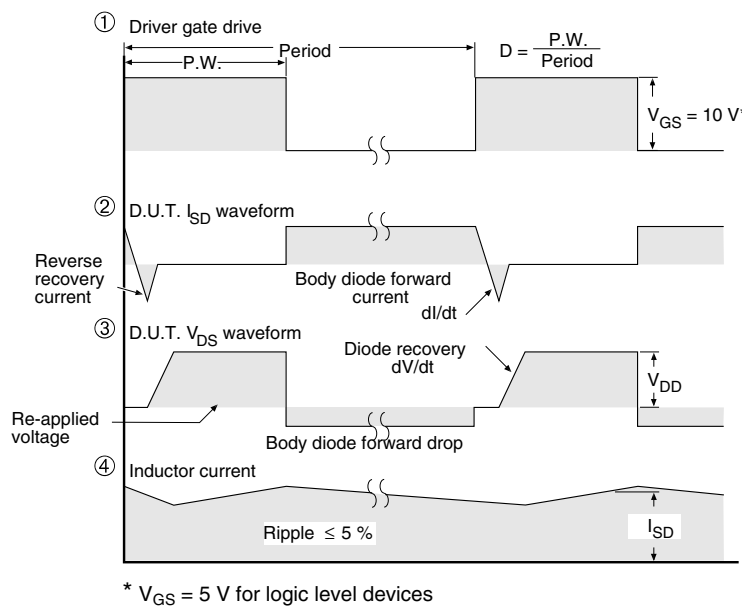
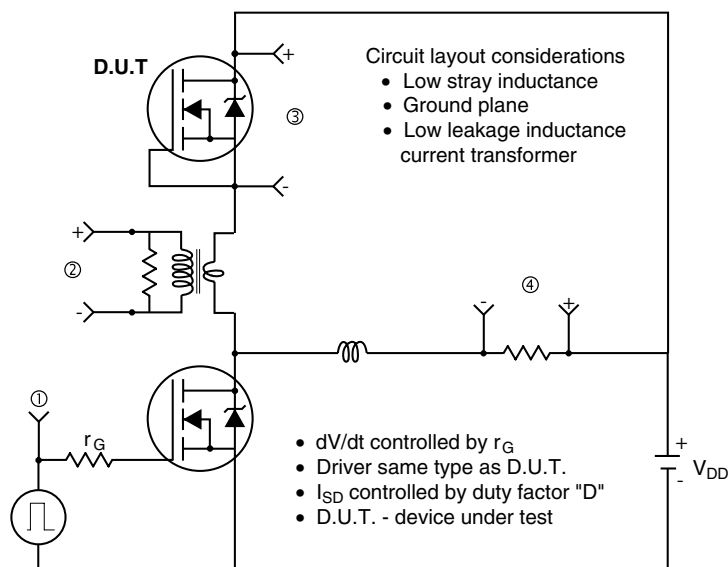


Fig. 16 - For N-Channel

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