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[Vishay/Siliconix](#)

[IRFPS38N60LPBF](#)

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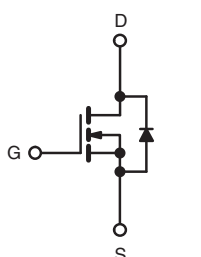
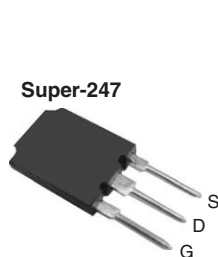
IRFPS38N60L, SiHFPS38N60L

Vishay Siliconix

Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.12
Q_g (Max.) (nC)	320	
Q_{gs} (nC)	85	
Q_{gd} (nC)	160	
Configuration	Single	



N-Channel MOSFET

FEATURES

- Superfast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simple Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free	IRFPS38N60LPbF
	SiHFPS38N60L-E3
SnPb	IRFPS38N60L
	SiHFPS38N60L

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	150	W/ $^\circ\text{C}$
Linear Derating Factor		4.3	
Single Pulse Avalanche Energy ^b	E_{AS}	680	mJ
Repetitive Avalanche Current ^a	I_{AR}	38	A
Repetitive Avalanche Energy ^a	E_{AR}	54	mJ
Maximum Power Dissipation	P_D	540	W
Peak Diode Recovery dV/dt ^c	dV/dt	19	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 12).
- Starting $T_J = 25^\circ\text{C}$, $L = 0.91\text{ mH}$, $R_g = 25\ \Omega$, $I_{AS} = 38\text{ A}$, $dV/dt = 13\text{ V/ns}$ (see fig. 14a).
- $I_{SD} \leq 38\text{ A}$, $dI/dt \leq 630\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.22	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	410	-	mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	2.0	mA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 23 A ^b	-	0.12	0.15	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 23 A ^b		20	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	7990	-	pF
Output Capacitance	C _{oss}			-	740	-	
Reverse Transfer Capacitance	C _{rss}			-	72	-	
Effective Output Capacitance	C _{oss eff.}	V _{GS} = 0 V V _{DS} = 0 V to 480 V ^c		-	350	-	
Effective Output Capacitance (Energy Related)	C _{oss eff. (ER)}			-	260	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 38 A, V _{DS} = 480 V see fig. 7 and 15 ^b	-	-	320	nC
Gate-Source Charge	Q _{gs}			-	-	85	
Gate-Drain Charge	Q _{gd}			-	-	160	
Gate Resistance	R _G	f = 1 MHz, open drain		-	1.2	-	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 38 A, R _G = 4.3 Ω, V _{GS} = 10 V, see fig. 11a and 11b ^b		-	44	-	ns
Rise Time	t _r			-	130	-	
Turn-Off Delay Time	t _{d(off)}			-	92	-	
Fall Time	t _f			-	69	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	38	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	150	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 38 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 38 A		-	170	250	ns
		T _J = 125 °C, dI/dt = 100 A/μs ^b		-	420	630	
Body Diode Reverse Recovery Charge	Q _{rr}	T _J = 25 °C, I _F = 38 A, V _{GS} = 0 V ^b		-	830	1240	nC
		T _J = 125 °C, dI/dt = 100 A/μs ^b		-	2600	3900	
Reverse Recovery Time	I _{RRM}	T _J = 25 °C		-	9.1	14	A
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 12).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

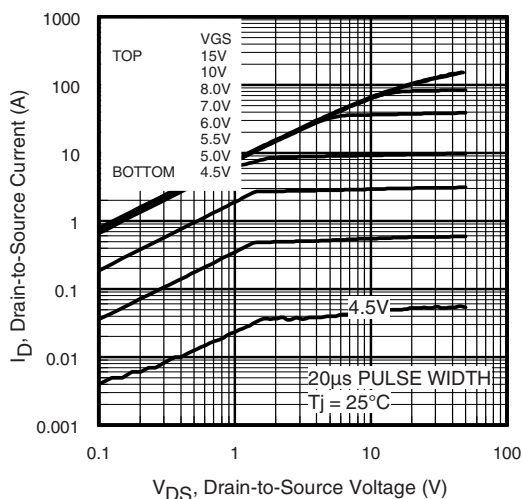


Fig. 1 - Typical Output Characteristics

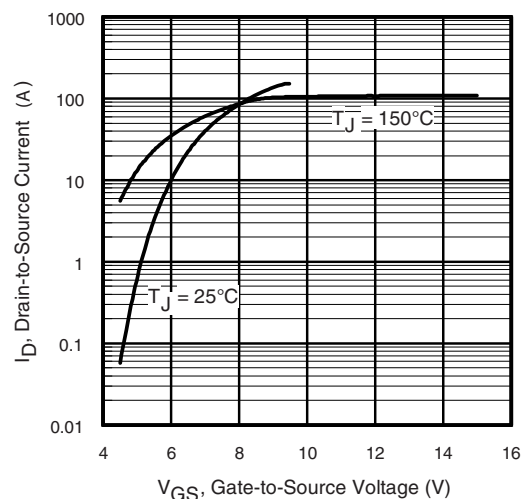


Fig. 3 - Typical Transfer Characteristics

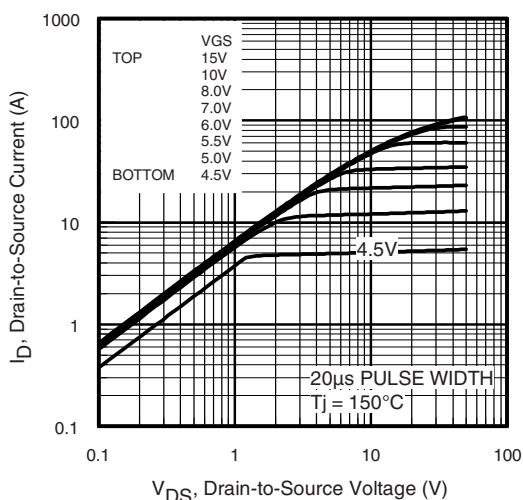


Fig. 2 - Typical Output Characteristics

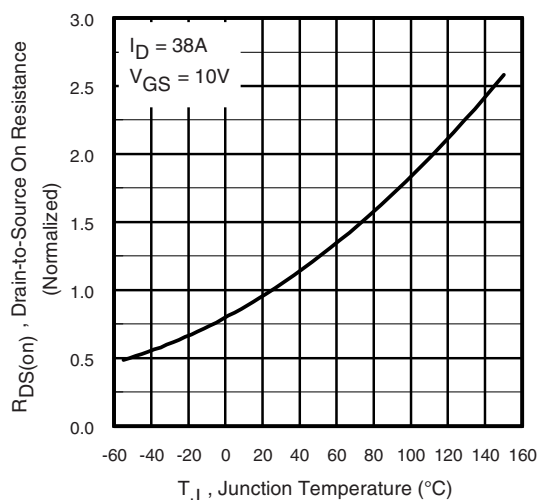


Fig. 4 - Normalized On-Resistance vs. Temperature

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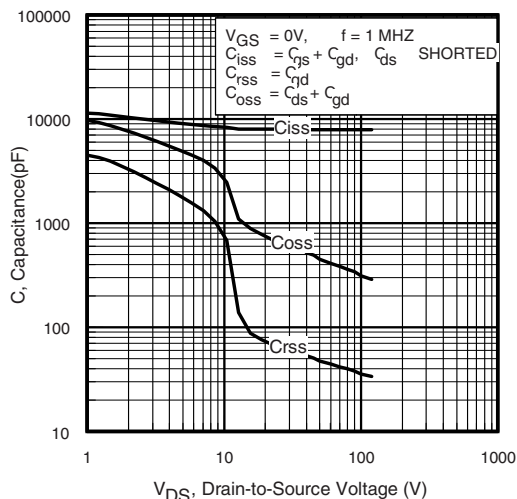


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

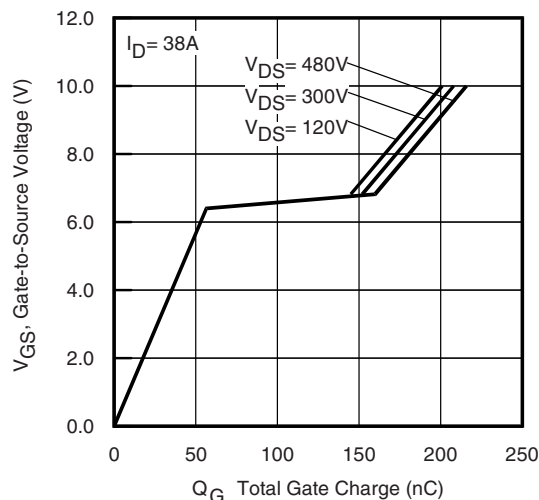


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

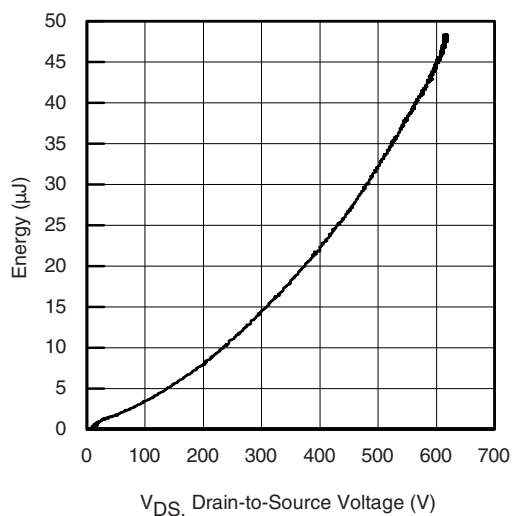


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

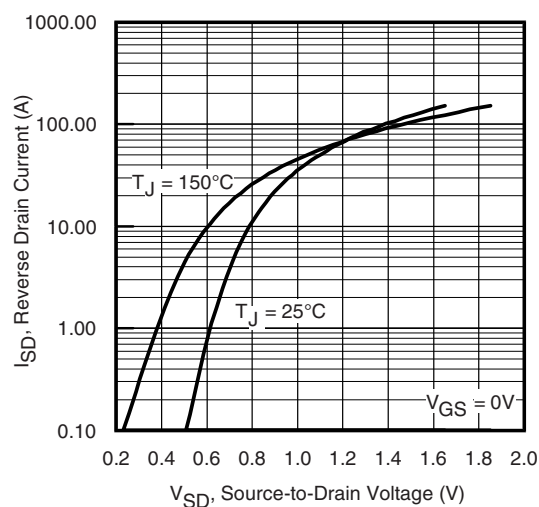


Fig. 8 - Typical Source-Drain Diode Forward Voltage



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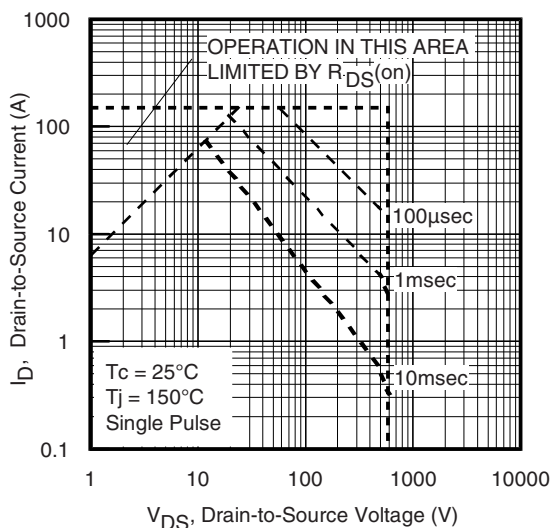


Fig. 9 - Maximum Safe Operating Area

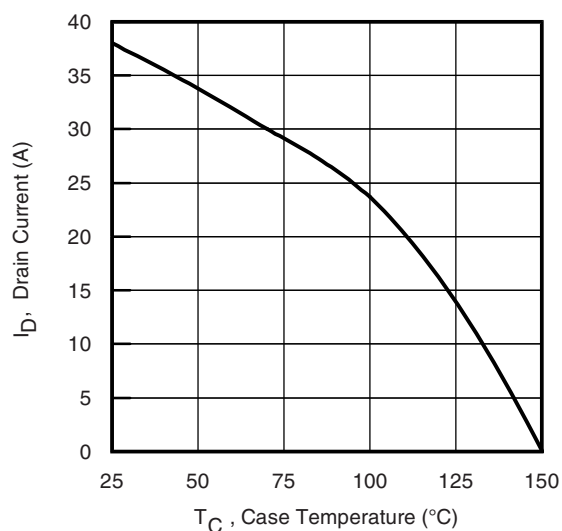


Fig. 10 - Maximum Drain Current vs. Case Temperature

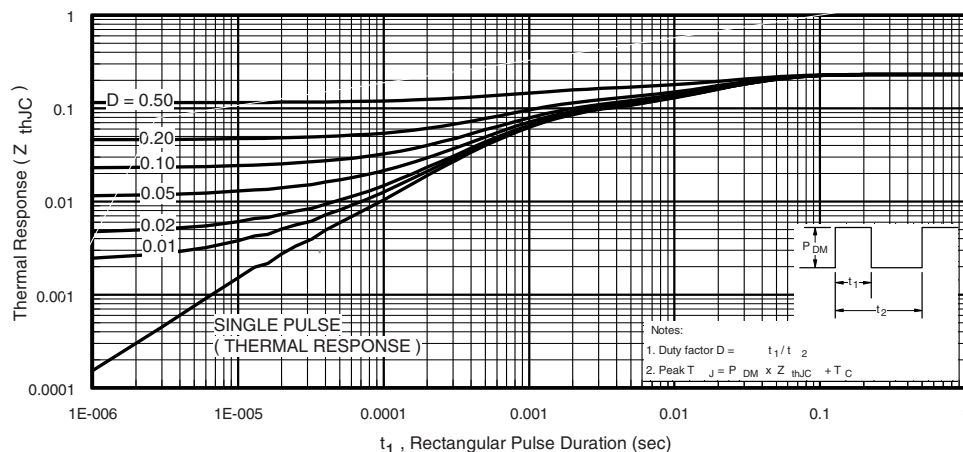


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

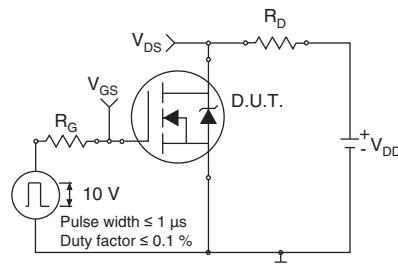


Fig. 11a - Switching Time Test Circuit

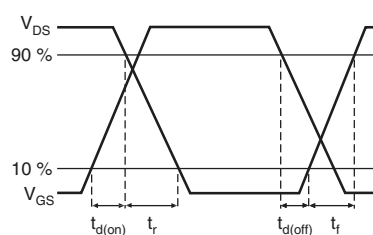


Fig. 11b - Switching Time Waveforms

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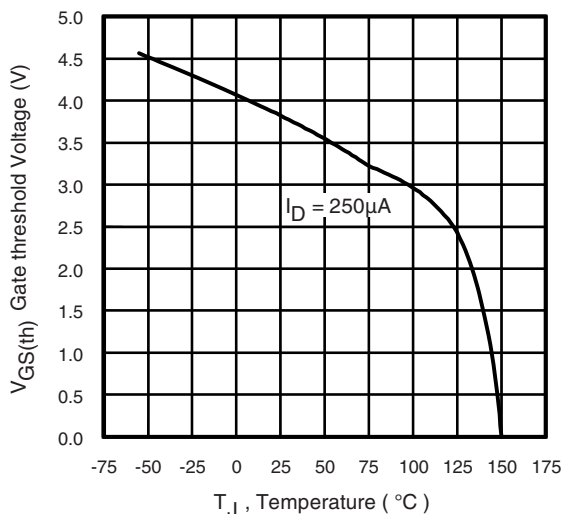


Fig. 13 - Threshold Voltage vs. Temperature

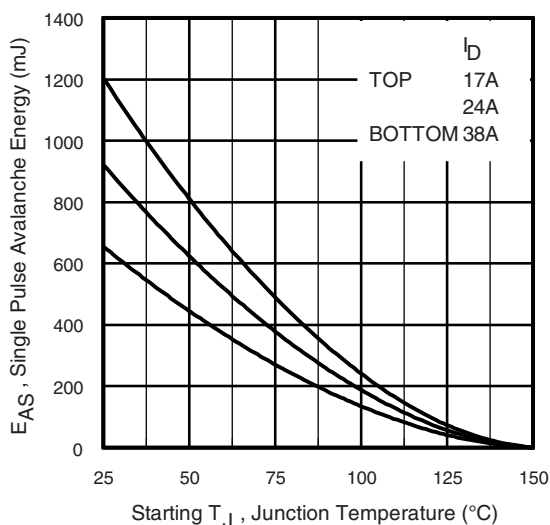


Fig. 14a - Maximum Avalanche Energy vs. Drain Current

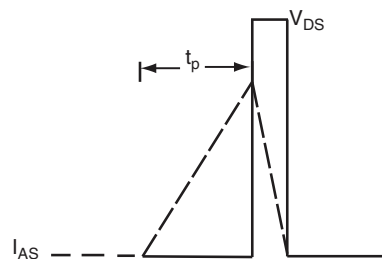


Fig. 14c - Unclamped Inductive Waveforms

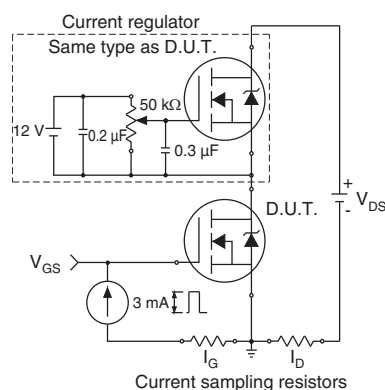


Fig. 15a - Basic Gate Charge Waveform

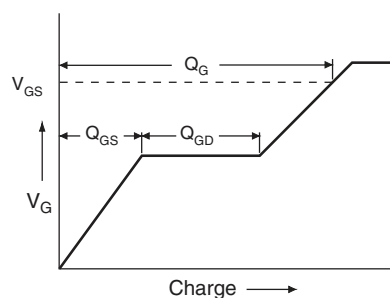


Fig. 15b - Gate Charge Test Circuit

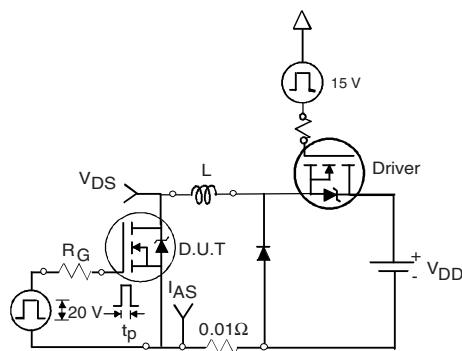


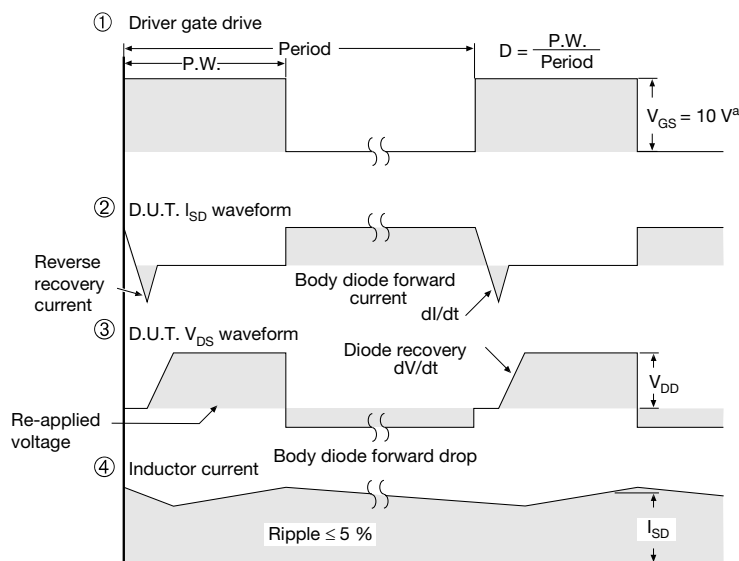
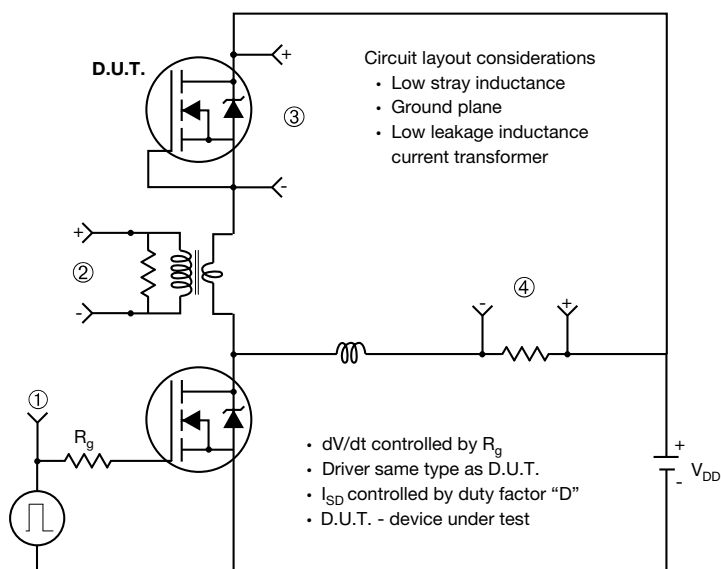
Fig. 14b - Unclamped Inductive Test Circuit



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Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 16 - For N-Channel

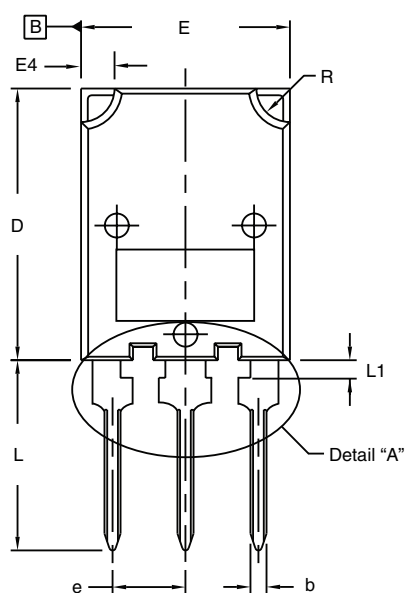
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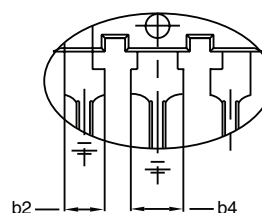
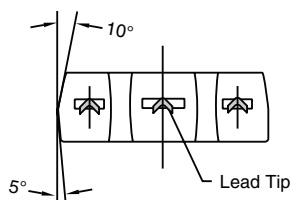
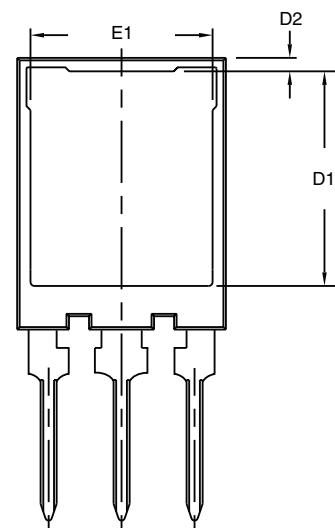
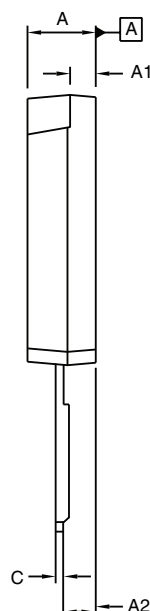
Package Information

Vishay Siliconix

TO-274AA (HIGH VOLTAGE)



⌀ 0.10 (0.25) ⌀ B A ⌀



Detail "A"
Scale: 2:1

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c	0.80	1.20	0.031	0.047
D	19.80	20.80	0.780	0.819

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

ECN: S-82247-Rev. A, 06-Oct-08
DWG: 5975

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body.
3. Outline conforms to JEDEC outline to TO-274AA.



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