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[International Rectifier \(Infineon Technologies Americas Corp.\)](#)
[IRF6215SPBF](#)

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sales@integrated-circuit.com

International
IR Rectifier

PD - 95132

IRF6215S/LPbF

- Lead-Free
- Advanced Process Technology
- Surface Mount (IRF6215S)
- Low-profile through-hole (IRF6215L)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF6215L) is available for low-profile applications.

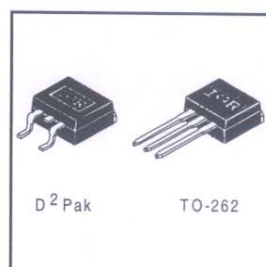
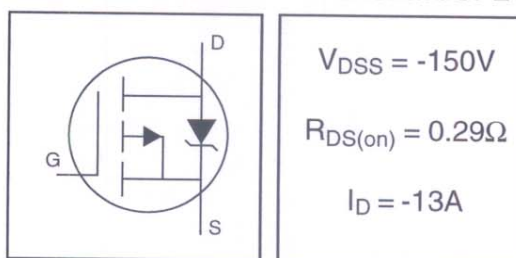
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -10V ^⑤	-13	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -10V ^⑤	-9.0	
I_{DM}	Pulsed Drain Current ^{① ⑤}	-44	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation	3.8	W
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^{② ⑤}	310	mJ
I_{AR}	Avalanche Current ^①	-6.6	A
E_{AR}	Repetitive Avalanche Energy ^①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ^{③ ⑤}	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	—	40	

HEXFET® Power MOSFET



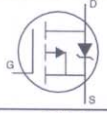
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-150	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.29	Ω	$V_{GS} = -10V$, $I_D = -6.6A$ ④
		—	—	0.58		$V_{GS} = -10V$, $I_D = -6.6A$ ④ $T_J = 150^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	3.6	—	—	S	$V_{DS} = -25V$, $I_D = -6.6A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = 150V$, $V_{GS} = 0V$
		—	—	-250		$V_{DS} = 120V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	—	66	nC	$I_D = -6.6A$
Q_{gs}	Gate-to-Source Charge	—	—	8.1		$V_{DS} = -120V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	35		$V_{GS} = -10V$, See Fig. 6 and 13 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	14	—		$V_{DD} = -75V$
t_r	Rise Time	—	36	—		$I_D = -6.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	53	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	37	—		$R_D = 12\Omega$, See Fig. 10 ④ ⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	860	—		$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	220	—	pF	$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	130	—		$f = 1.0MHz$, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-44		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	$T_J = 25^\circ\text{C}$, $I_S = -6.6A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	160	240	ns	$T_J = 25^\circ\text{C}$, $I_F = -6.6A$
Q_{rr}	Reverse Recovery Charge	—	1.2	1.7	μC	$di/dt = -100A/\mu s$ ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 14mH$
 $R_G = 25\Omega$, $I_{AS} = -6.6A$. (See Figure 12)
- ③ $I_{SD} \leq -6.6A$, $di/dt \leq -620A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRF6215 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

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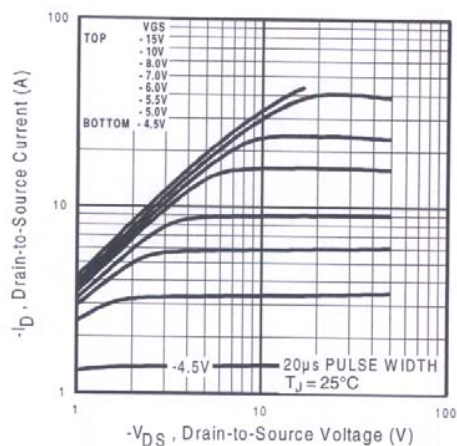


Fig 1. Typical Output Characteristics

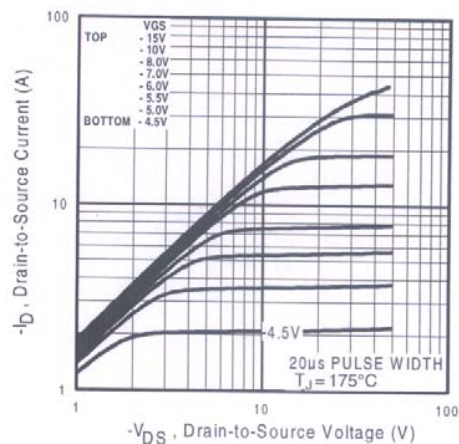


Fig 2. Typical Output Characteristics

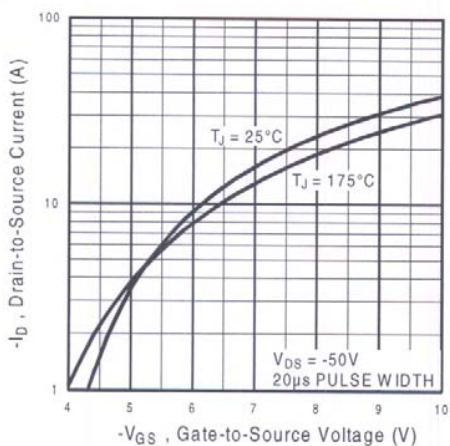


Fig 3. Typical Transfer Characteristics

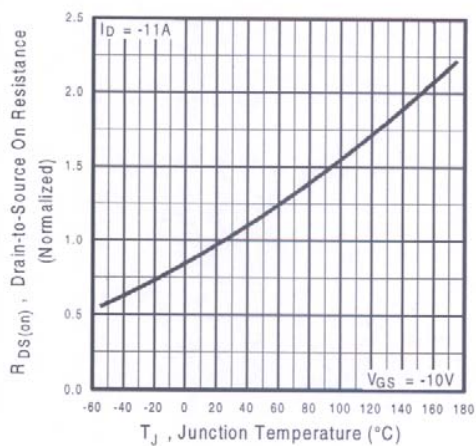


Fig 4. Normalized On-Resistance
Vs. Temperature

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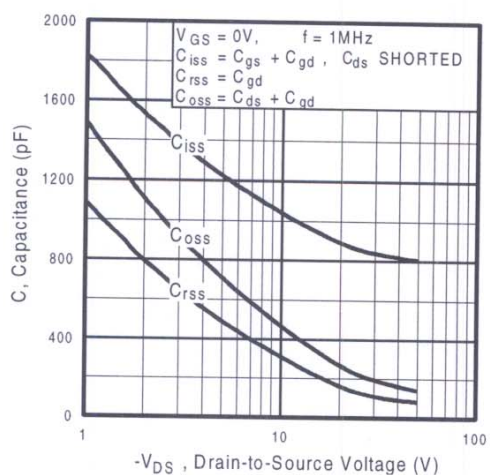


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

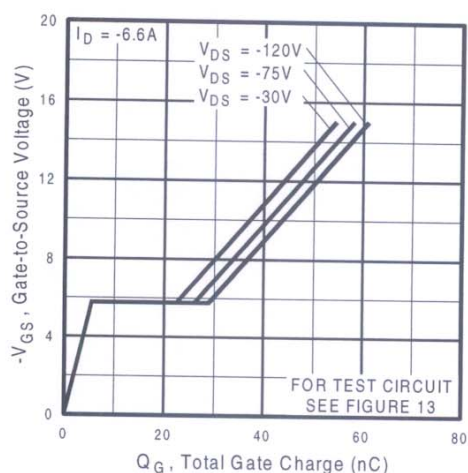


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

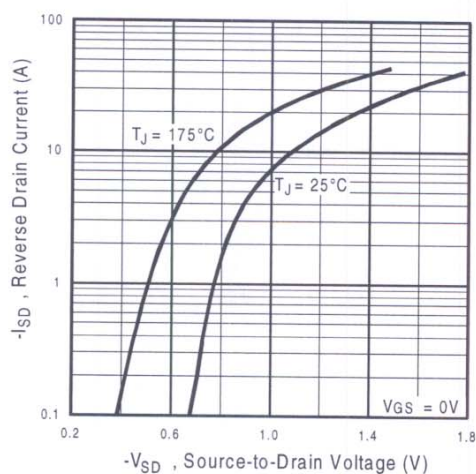


Fig 7. Typical Source-Drain Diode Forward Voltage

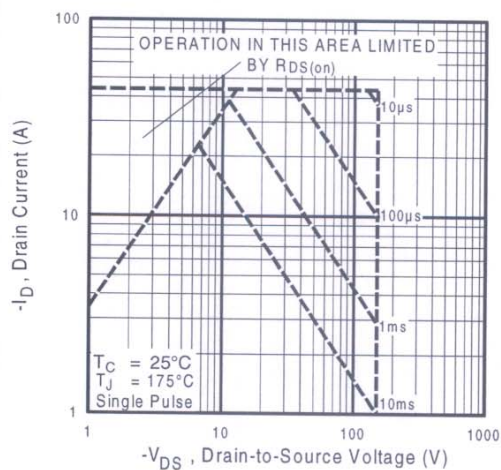


Fig 8. Maximum Safe Operating Area

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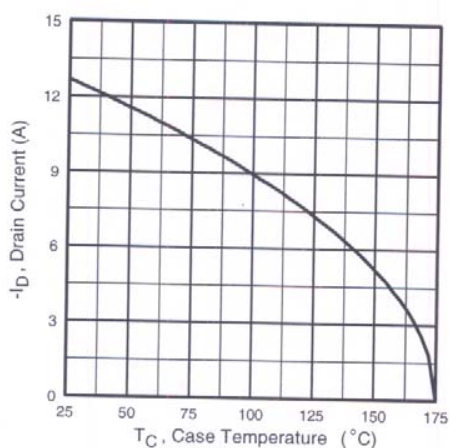


Fig 9. Maximum Drain Current Vs. Case Temperature

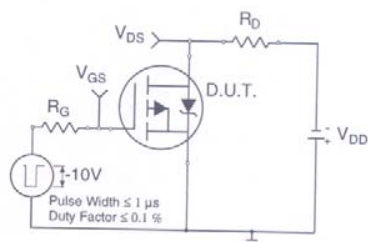


Fig 10a. Switching Time Test Circuit

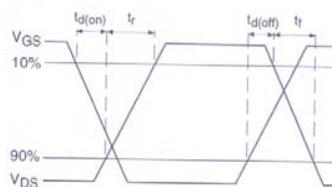


Fig 10b. Switching Time Waveforms

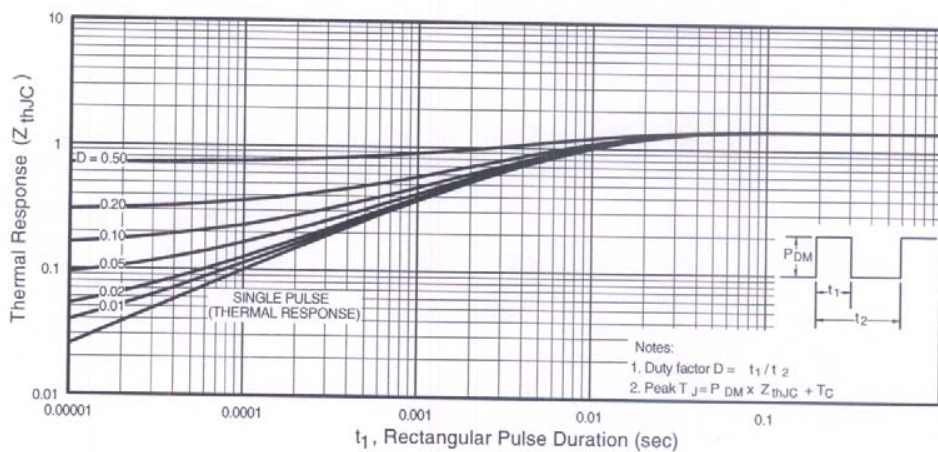


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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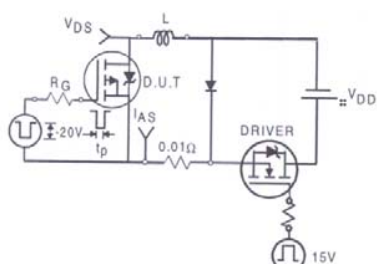


Fig 12a. Unclamped Inductive Test Circuit

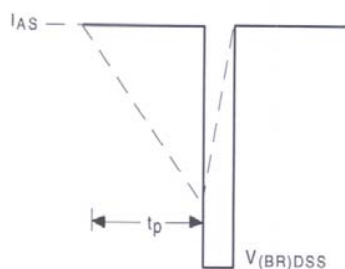


Fig 12b. Unclamped Inductive Waveforms

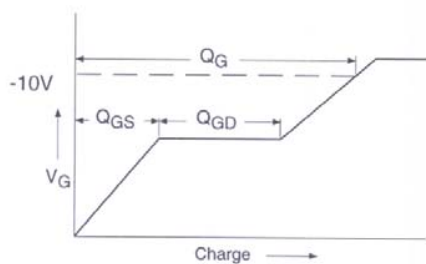


Fig 13a. Basic Gate Charge Waveform

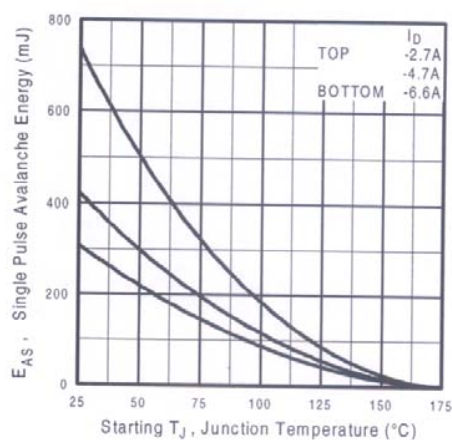


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

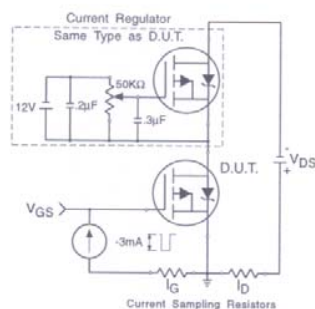
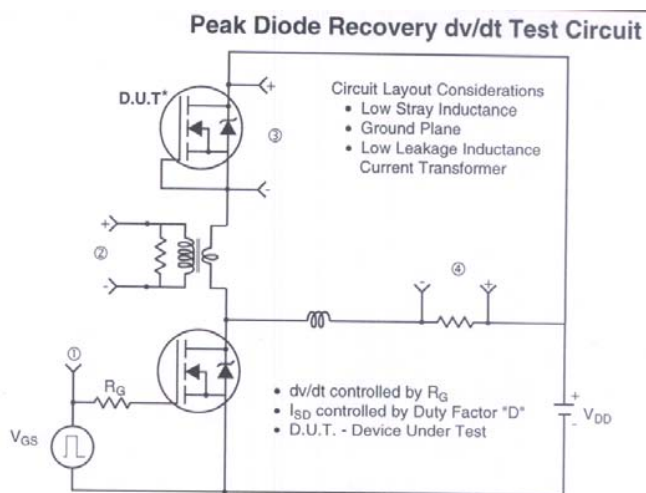


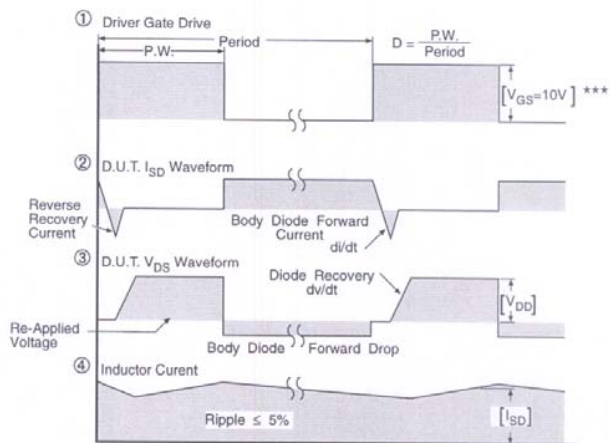
Fig 13b. Gate Charge Test Circuit

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* Reverse Polarity of D.U.T. for P-Channel



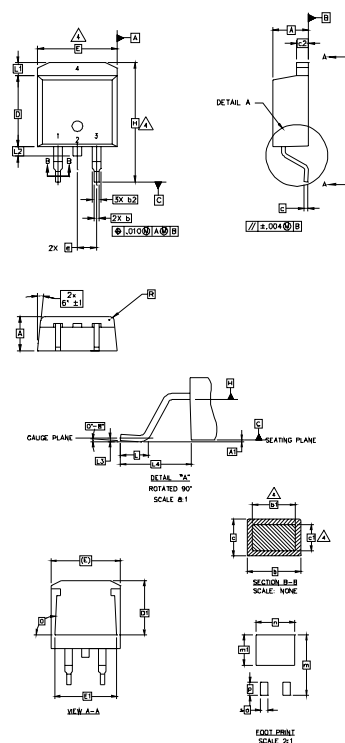
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

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D²Pak Package Outline



NOTES

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

S Y M B O L	5. CONTROLLING DIMENSION: INCH.						N O T E S
	DIMENSIONS						
	MILLIMETERS		INCHES				
A	MIN.	MAX.	MIN.	MAX.			
A	4.06	4.83	.160	.190			
A1	0.00	0.254	.000	.010			
b	0.51	.099	.020	.039			
b1	0.51	.089	.020	.035			4
b2	1.14	1.78	.045	.070			
c	0.38	0.74	.015	.029			
c1	0.38	0.58	.015	.023			
C	1.14	1.65	.045	.065			
D	8.51	9.65	.335	.380			3
D1	6.86		.270				
E	10.67		.420				420
E1	6.22		.245				
e	2.54 BSC		.100 BSC				
H	14.61	15.88	.575	.625			
L	1.78	2.79	.070	.110			
L1			.065	.165			
L2	1.27	1.78	.050	.070			
L3	.025 BSC		.010 BSC				
L4	4.78	5.28	.188	.208			
Lm	17.78		.700				
m	8.89		.350				
n	11.43		.450				
o	2.08		.082				
p	3.81		.150				
R	0.51	0.71	.020	.028			
Ø	90°	93°	90°	93°			

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
2, 4.- DRAIN
3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
2, 4.- COLLECTOR
3.- EMITTER

DIODES

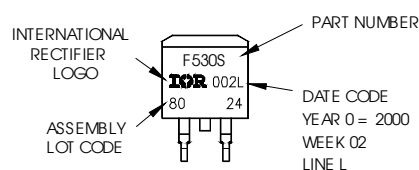
- 1.- ANODE •
2, 4.- CATHODE
3.- ANODE

* PART DEPENDENT.

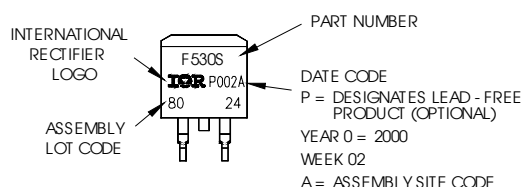
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"



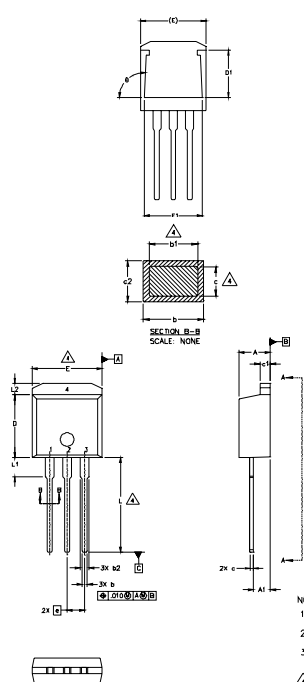
OR



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TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

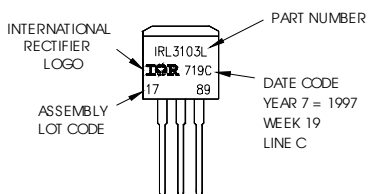
LEAD ASSIGNMENTS

IGBT
HEXFET
1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- DRAIN

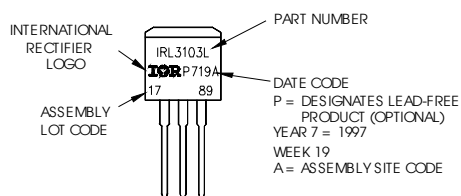
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4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line position indicates "Lead-Free"



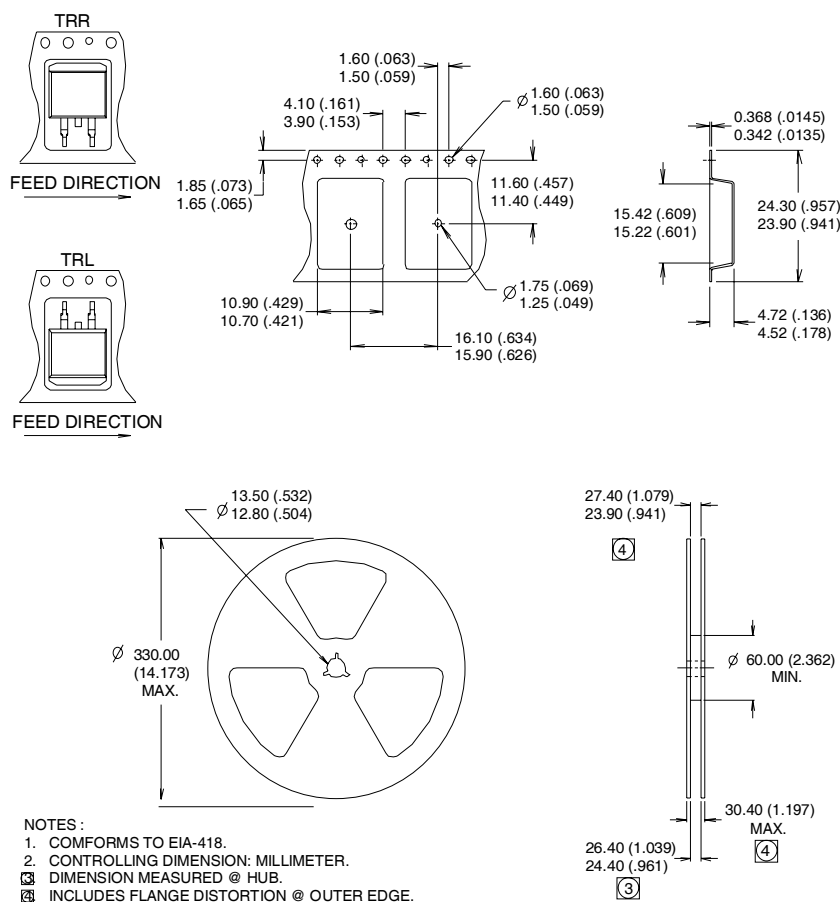
OR



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D²Pak Tape & Reel Information



Data and specifications subject to change without notice.

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Note: For the most current drawings please refer to the IR website at:

<http://www.irf.com/package/>