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[IRL3502SPBF](#)

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# IRL3502SPbF

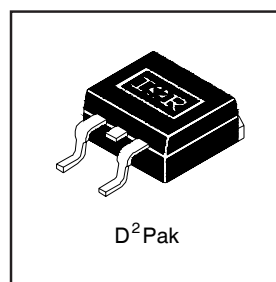
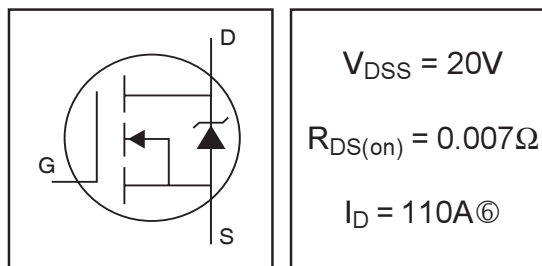
HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching
- Lead-Free

## Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters in the PC environment. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.



## Absolute Maximum Ratings

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 4.5VⓈ	110Ⓢ	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 4.5VⓈ	67	
I <sub>DM</sub>	Pulsed Drain Current ①Ⓢ	420	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	140	W
	Linear Derating Factor	1.1	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 10	V
V <sub>GSM</sub>	Gate-to-Source Voltage (Start Up Transient, t <sub>p</sub> = 100μs)	14	V
E <sub>AS</sub>	Single Pulse Avalanche Energy②Ⓢ	390	mJ
I <sub>AR</sub>	Avalanche Current①	64	A
E <sub>AR</sub>	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③Ⓢ	5.0	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	---	0.89	°C/W
R <sub>θJA</sub>	Junction-to-Ambient ( PCB Mounted, steady-state)**	---	40	

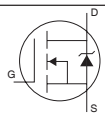
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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.019	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1.0\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.008	$\Omega$	$V_{GS} = 4.5V, I_D = 64A$ ④
		—	—	0.007		$V_{GS} = 7.0V, I_D = 64A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	77	—	—	S	$V_{DS} = 10V, I_D = 64A$ ⑤
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 10V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
$Q_g$	Total Gate Charge	—	—	110	nC	$I_D = 64A$
$Q_{gs}$	Gate-to-Source Charge	—	—	27		$V_{DS} = 16V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	39		$V_{GS} = 4.5V$ , See Fig. 6 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 10V$ $I_D = 64A$ $R_G = 3.8\Omega, V_{GS} = 4.5V$ $R_D = 0.15\Omega$ , ④ ⑤
$t_r$	Rise Time	—	140	—		
$t_{d(off)}$	Turn-Off Delay Time	—	96	—		
$t_f$	Fall Time	—	130	—		
$L_S$	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
$C_{iss}$	Input Capacitance	—	4700	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0\text{MHz}$ , See Fig. 5 ⑤
$C_{oss}$	Output Capacitance	—	1900	—		
$C_{riss}$	Reverse Transfer Capacitance	—	640	—		

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	110 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ① ⑤	—	—	420		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 64A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	87	130	ns	$T_J = 25^\circ\text{C}, I_F = 64A$
$Q_{rr}$	Reverse Recovery Charge	—	200	310	nC	$di/dt = 100A/\mu s$ ④ ⑤
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 190\mu\text{H}$   
 $R_G = 25\Omega, I_{AS} = 64A$ .
- ③  $I_{SD} \leq 64A, di/dt \leq 86A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ Uses IRL3502 data and test conditions
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

\*\* When mounted on FR-4 board using minimum recommended footprint.

For recommended footprint and soldering techniques refer to application note #AN-994.

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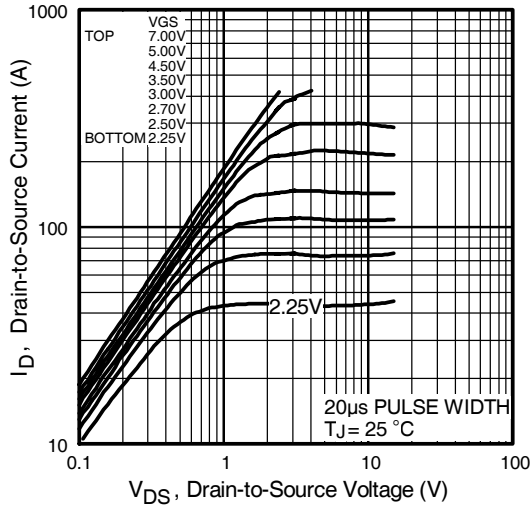


Fig 1. Typical Output Characteristics

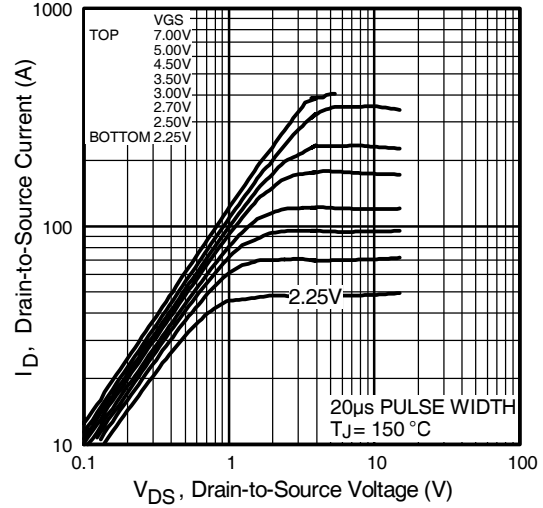


Fig 2. Typical Output Characteristics

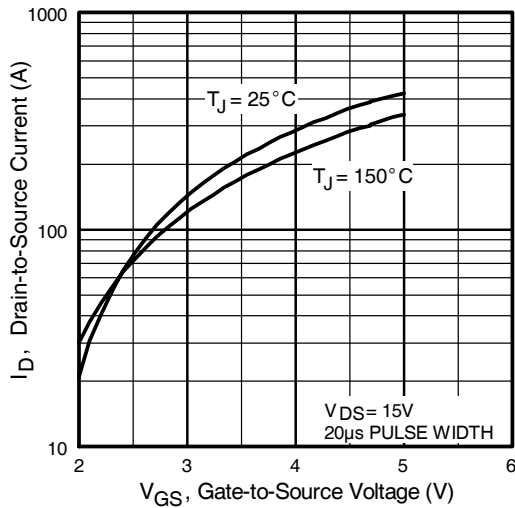


Fig 3. Typical Transfer Characteristics

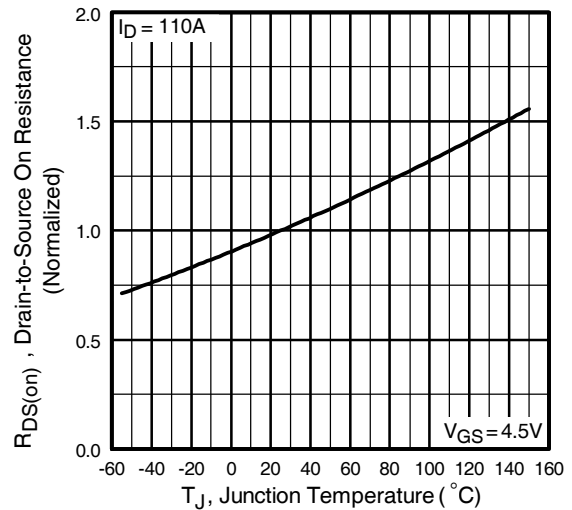
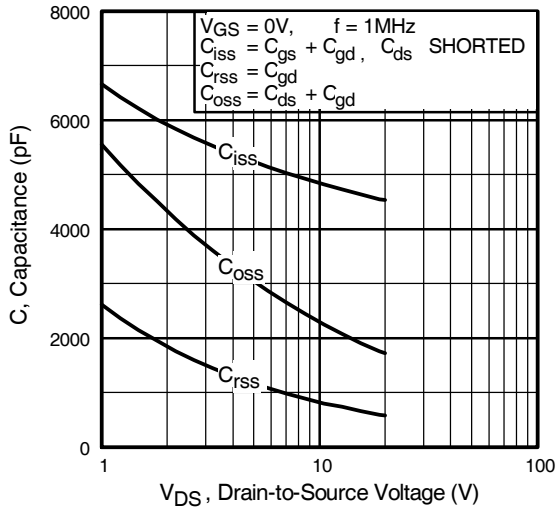


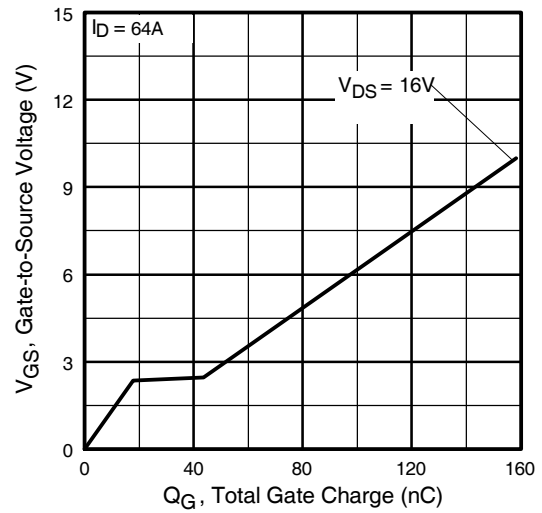
Fig 4. Normalized On-Resistance Vs. Temperature

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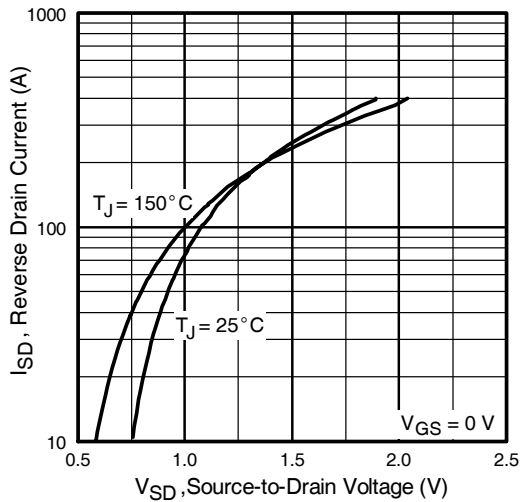
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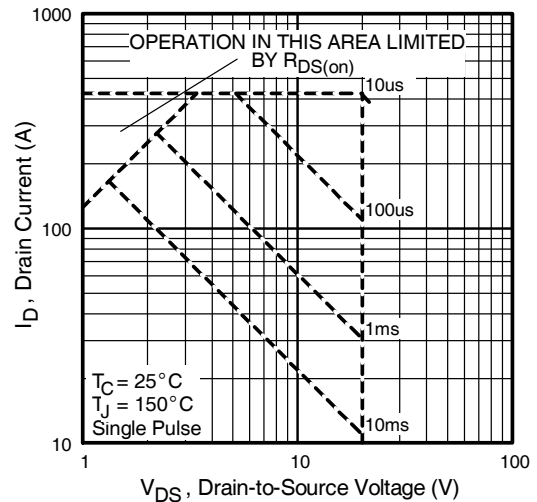
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



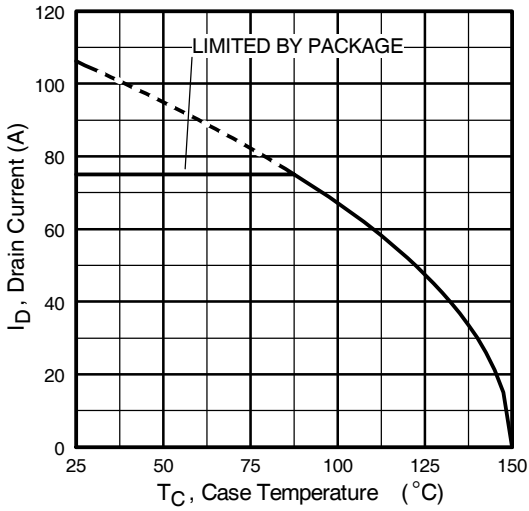
**Fig 7.** Typical Source-Drain Diode Forward Voltage



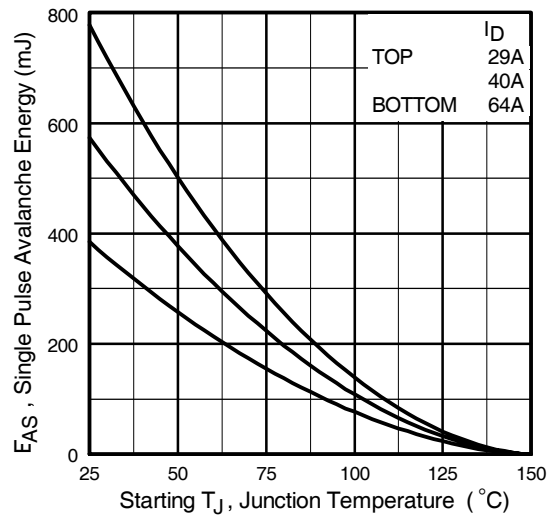
**Fig 8.** Maximum Safe Operating Area

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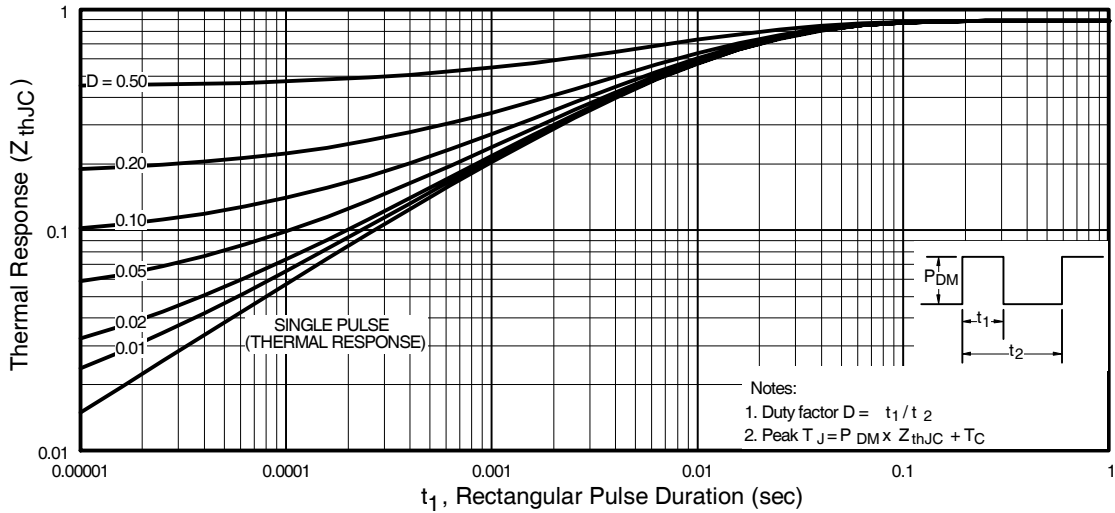
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**Fig 9.** Maximum Drain Current Vs. Case Temperature



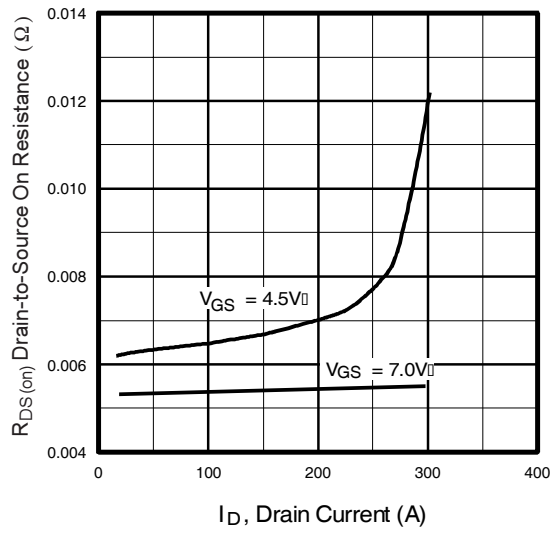
**Fig 10.** Maximum Avalanche Energy Vs. Drain Current



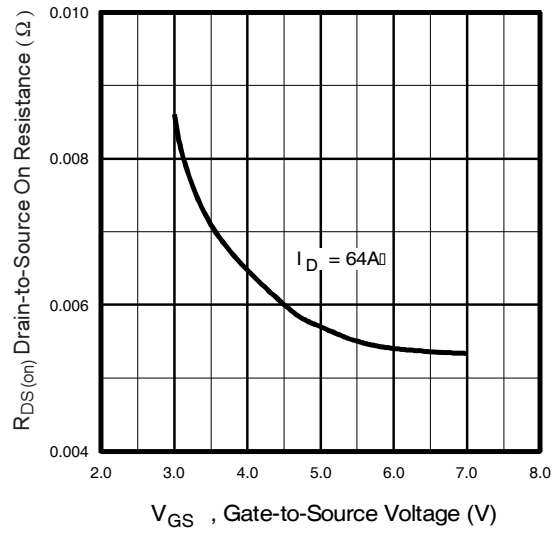
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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**Fig 12.** On-Resistance Vs. Drain Current



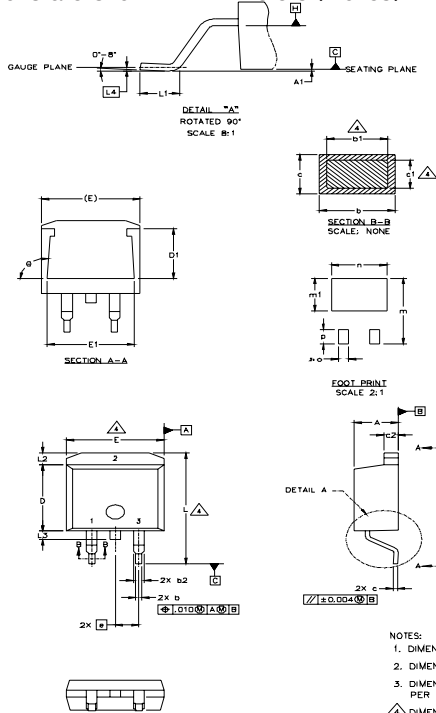
**Fig 13.** On-Resistance Vs. Gate Voltage

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## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	3
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25	BSC	.010	BSC	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

**LEAD ASSIGNMENTS**

HEXFET	IGBTs, CoPACK	DIODES
1- GATE	1- GATE	1- ANODE
2- DRAIN	2- COLLECTOR	2- CATHODE
3- SOURCE	3- EMITTER	3- ANODE

\* PART DEPENDENT.

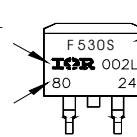
- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994  
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]  
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.  
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.  
 5. CONTROLLING DIMENSION: INCH.

## D<sup>2</sup>Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH  
 LOT CODE 8024  
 ASSEMBLED ON WW 02, 2000  
 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line  
 position indicates "Lead-Free"

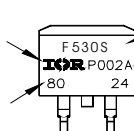
INTERNATIONAL  
 RECTIFIER  
 LOGO  
 ASSEMBLY  
 LOT CODE



PART NUMBER  
 DATE CODE  
 YEAR 0 = 2000  
 WEEK 02  
 LINE L

**OR**

INTERNATIONAL  
 RECTIFIER  
 LOGO  
 ASSEMBLY  
 LOT CODE



PART NUMBER  
 DATE CODE  
 P = DESIGNATES LEAD-FREE  
 PRODUCT (OPTIONAL)  
 YEAR 0 = 2000  
 WEEK 02  
 A = ASSEMBLY SITE CODE

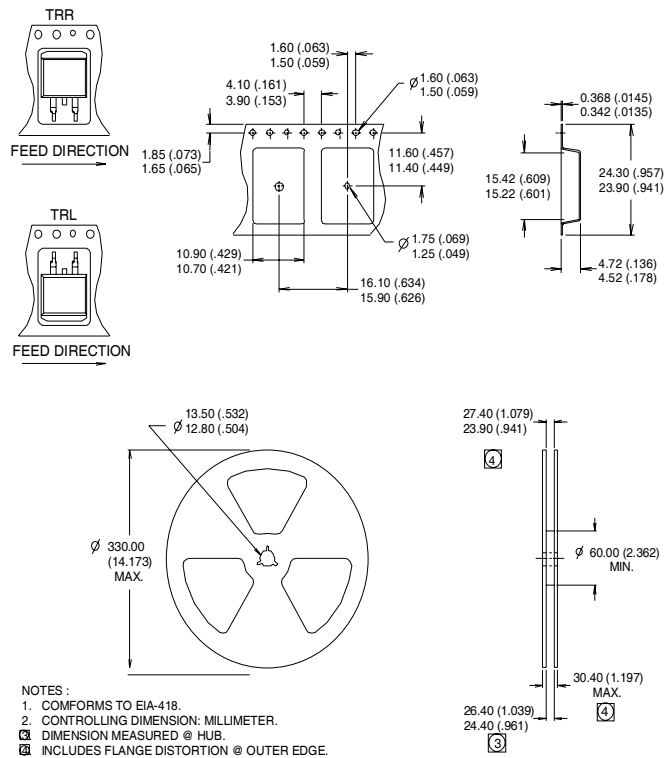


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## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Data and specifications subject to change without notice.

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<http://www.irf.com/package/>