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[Vishay Semiconductor/Diodes Division](#)
[VS-8TQ100SPBF](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



www.vishay.com

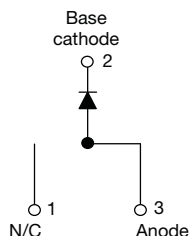
VS-8TQ080SPbF, VS-8TQ100SPbF

Vishay Semiconductors

High Performance Schottky Rectifier, 8 A



TO-263AB (D²PAK)



FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- High frequency operation
- High purity, high temperature epoxy encapsulation for enhanced mechanical strength and moisture resistance
- Guard ring for enhanced ruggedness and long term reliability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- AEC-Q101 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY

Package	TO-263AB (D ² PAK)
I _{F(AV)}	8 A
V _R	80 V, 100 V
V _F at I _F	0.72 V
I _{RM} max.	7 mA at 125 °C
T _J max.	175 °C
Diode variation	Single die
E _{AS}	7.5 mJ

DESCRIPTION

The VS-8TQ... Schottky rectifier series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in switching power supplies, converters, freewheeling diodes, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
I _{F(AV)}	Rectangular waveform	8	A
V _{RRM}	Range	80, 100	V
I _{FSM}	t _p = 5 μs sine	850	A
V _F	8 A _{pk} , T _J = 125 °C	0.58	V
T _J	Range	-55 to +175	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	VS-8TQ080SPbF	VS-8TQ100SPbF	UNITS
Maximum DC reverse voltage	V _R	80	100	V
Maximum working peak reverse voltage	V _{RWM}			

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current See fig. 5	I _{F(AV)}	50 % duty cycle at T _C = 157 °C, rectangular waveform	8	A
Maximum peak one cycle non-repetitive surge current See fig. 7	I _{FSM}	5 μs sine or 3 μs rect. pulse	850	A
		10 ms sine or 6 ms rect. pulse	230	
Non-repetitive avalanche energy	E _{AS}	T _J = 25 °C, I _{AS} = 0.50 A, L = 60 mH	7.50	mJ
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T _J maximum V _A = 1.5 x V _R typical	0.50	A



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ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop See fig. 1	V _{FM} ⁽¹⁾	8 A	T _J = 25 °C	0.72	V
		16 A		0.88	
		8 A	T _J = 125 °C	0.58	
		16 A		0.69	
Maximum reverse leakage current See fig. 2	I _{RM} (1)	T _J = 25 °C	V _R = Rated V _R	0.55	mA
		T _J = 125 °C		7	
Maximum junction capacitance	C _T	V _R = 5 V _{DC} (test signal range 100 kHz to 1 MHz), 25 °C		500	pF
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		8	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/μs

Note

(1) Pulse width < 300 μ s, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range		T _J , T _{Stg}		-55 to +175	°C
Maximum thermal resistance, junction to case		R _{thJC}	DC operation See fig. 4	2.0	°C/W
Typical thermal resistance, case to heatsink		R _{thCS}	Mounting surface, smooth and greased	0.50	
Approximate weight				2	g
				0.07	oz.
Mounting torque	minimum			6 (5)	kgf · cm (lbf · in)
	maximum			12 (10)	
Marking device		Case style D ² PAK	8TQ080S		
			8TQ100S		



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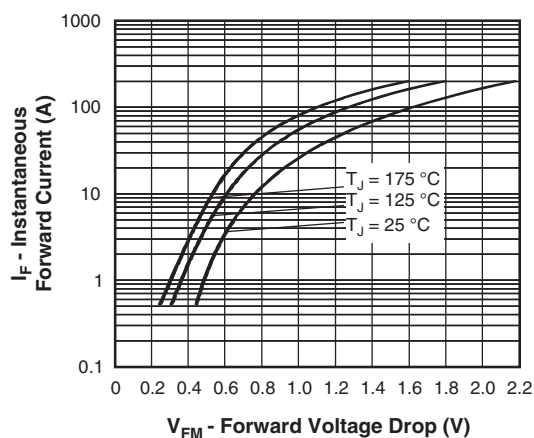


Fig. 1 - Maximum Forward Voltage Drop Characteristics

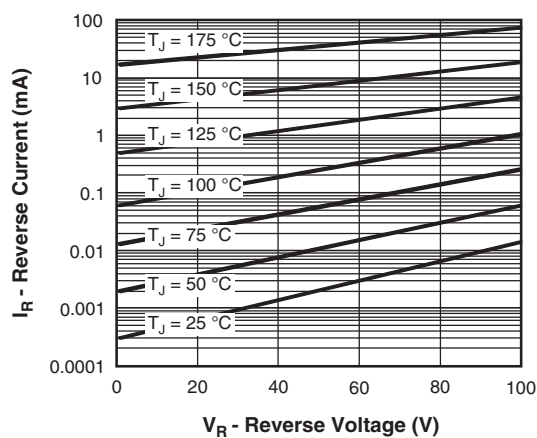


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

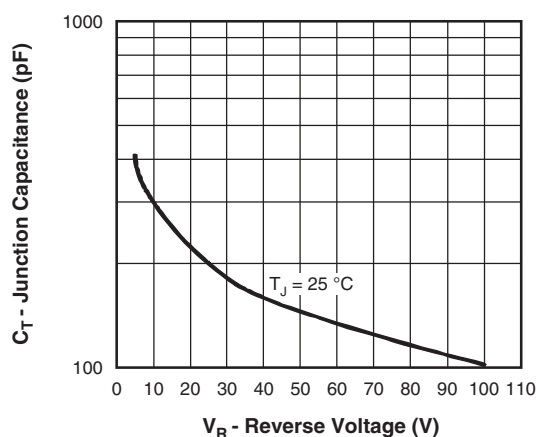


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

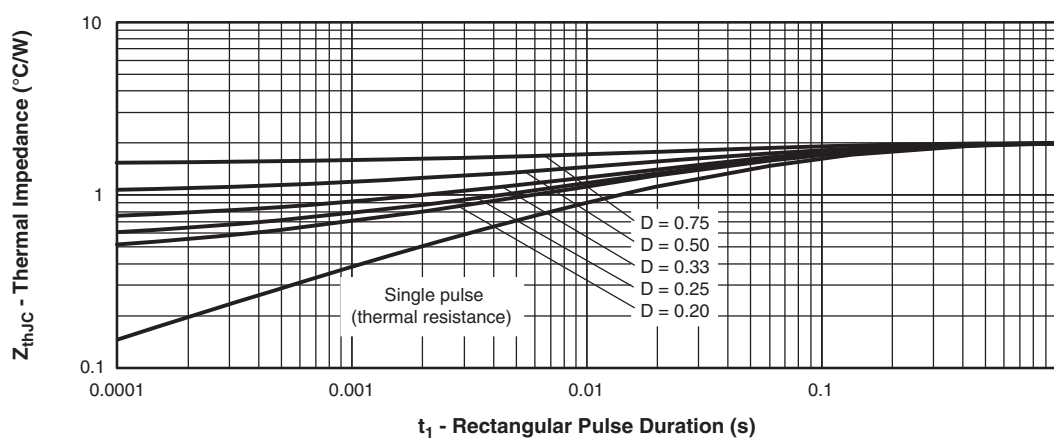


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics



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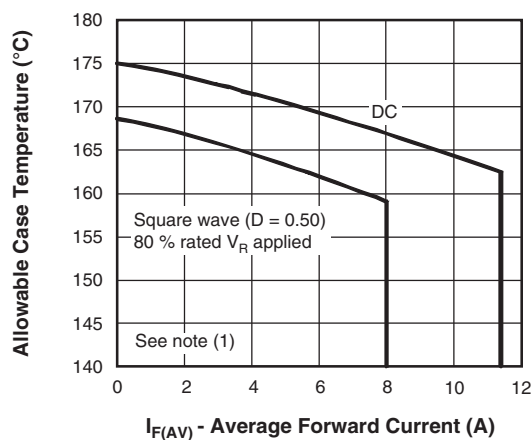


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

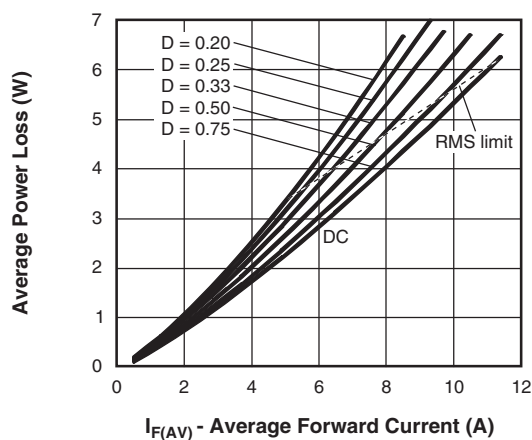


Fig. 6 - Forward Power Loss Characteristics

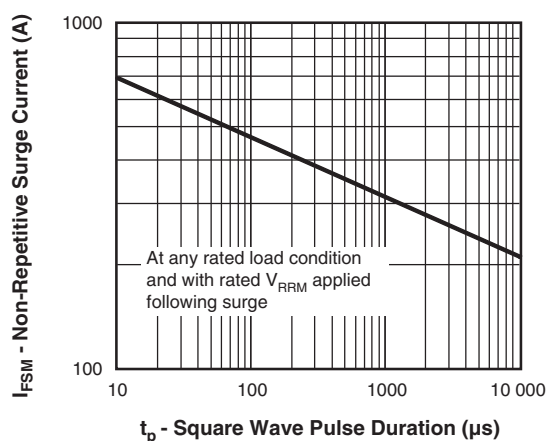


Fig. 7 - Maximum Non-Repetitive Surge Current

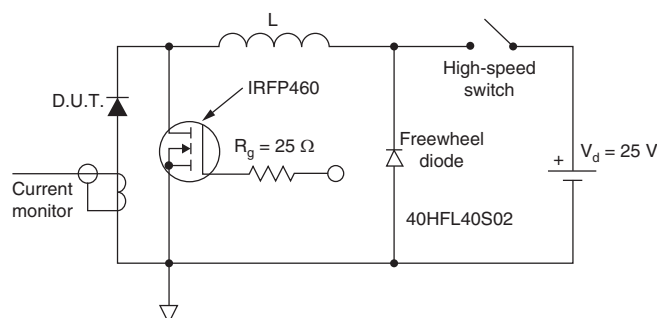


Fig. 8 - Unclamped Inductive Test Circuit

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$
 P_d = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 P_{dREV} = Inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R



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ORDERING INFORMATION TABLE

Device code	VS-	8	T	Q	100	S	TRL	PbF
	1	2	3	4	5	6	7	8
1	Vishay Semiconductors product							
2	Current rating (8 A)							
3	Circuit configuration: T = TO-220							
4	Schottky "Q" series							
5	Voltage ratings							
6	S = D ² PAK							
7	<ul style="list-style-type: none"> None = tube (50 pieces) TRL = tape and reel (left oriented) TRR = tape and reel (right oriented) 							
8	PbF = lead (Pb)-free							

080 = 80 V
100 = 100 V

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95046
Part marking information	www.vishay.com/doc?95054
Packaging information	www.vishay.com/doc?95032
SPICE models	www.vishay.com/doc?95291



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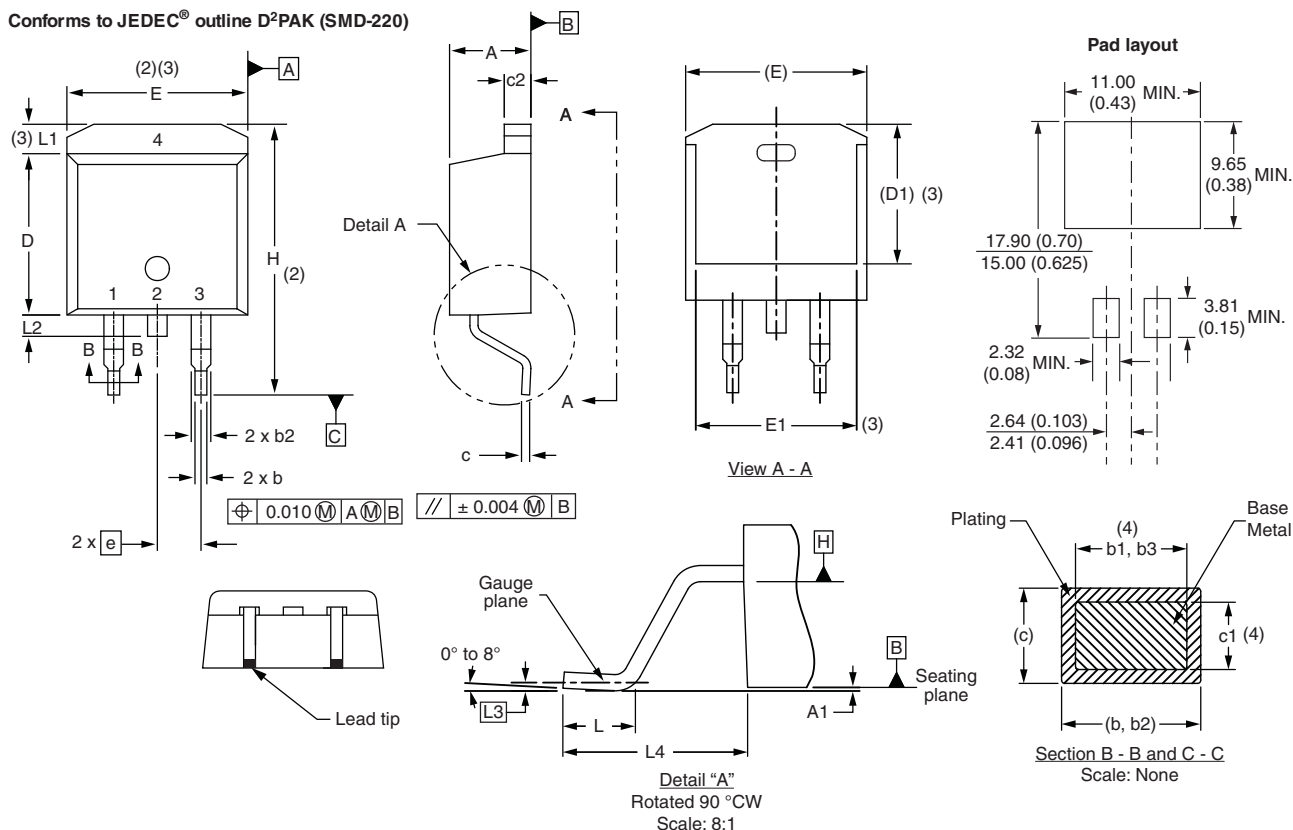
Outline Dimensions

Vishay Semiconductors

D²PAK

DIMENSIONS in millimeters and inches

Conforms to JEDEC® outline D²PAK (SMD-220)



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	0.00	0.254	0.000	0.010	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
H	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	-	0.066	3
L2	1.27	1.78	0.050	0.070	
L3	0.25 BSC		0.010 BSC		
L4	4.78	5.28	0.188	0.208	

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5 M-1994
- (2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
- (3) Thermal pad contour optional within dimension E, L1, D1 and E1
- (4) Dimension b1 and c1 apply to base metal only
- (5) Datum A and B to be determined at datum plane H
- (6) Controlling dimension: inch
- (7) Outline conforms to JEDEC® outline TO-263AB



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