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Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[International Rectifier \(Infineon Technologies Americas Corp.\)](#)
[IRG4BC40W-SPBF](#)

For any questions, you can email us directly:

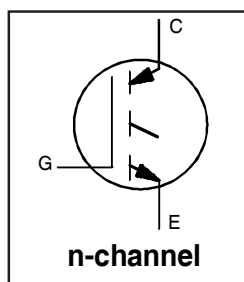
sales@integrated-circuit.com

International Rectifier

INSULATED GATE BIPOLAR TRANSISTOR

Features

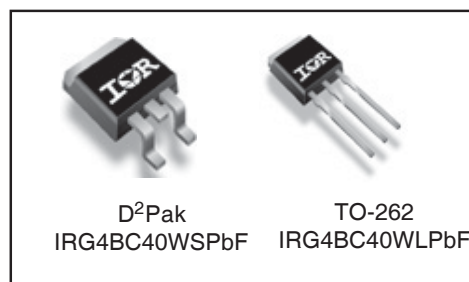
- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability
- Lead-Free



$V_{CES} = 600V$
$V_{CE(on)} \text{ typ.} = 2.05V$
@ $V_{GE} = 15V, I_C = 20A$

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >>300 kHz)



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	40	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	20	
I_{CM}	Pulsed Collector Current ①	160	
I_{LM}	Clamped Inductive Load Current ②	160	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	160	mJ
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	160	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	65	
T_J	Operating Junction and	-55 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.77	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted steady-state)	—	40	
Wt	Weight	2.0 (0.07)	—	g (oz)

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	$V_{GE} = 0V, I_C = 1.0A$
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.44	—	V/°C	$V_{GE} = 0V, I_C = 1.0mA$
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	2.05	2.5	V	$I_C = 20A, V_{GE} = 15V$
		—	2.36	—		$I_C = 40A, V_{GE} = 15V$
		—	1.90	—		$I_C = 20A, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	13	—	mV/°C	$V_{CE} = V_{GE}, I_C = 250\mu A$
g_{fe}	Forward Transconductance ⑤	18	28	—	S	$V_{CE} = 100V, I_C = 20A$
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 600V$
		—	—	2.0		$V_{GE} = 0V, V_{CE} = 10V, T_J = 25^\circ\text{C}$
		—	—	2500		$V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	98	147	nC	$I_C = 20A$
Q_{ge}	Gate - Emitter Charge (turn-on)	—	12	18		$V_{CC} = 400V$
Q_{gc}	Gate - Collector Charge (turn-on)	—	36	54		$V_{GE} = 15V$
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 20A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 10\Omega$ Energy losses include "tail" See Fig. 9, 10, 14
t_r	Rise Time	—	22	—		
$t_{d(off)}$	Turn-Off Delay Time	—	100	150		
t_f	Fall Time	—	74	110	mJ	$T_J = 150^\circ\text{C}$ $I_C = 20A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 10\Omega$ Energy losses include "tail" See Fig. 10, 11, 14
E_{on}	Turn-On Switching Loss	—	0.11	—		
E_{off}	Turn-Off Switching Loss	—	0.23	—		
E_{ts}	Total Switching Loss	—	0.34	0.45	nH	Measured 5mm from package
$t_{d(on)}$	Turn-On Delay Time	—	25	—		
t_r	Rise Time	—	23	—		
$t_{d(off)}$	Turn-Off Delay Time	—	170	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0MHz$
t_f	Fall Time	—	124	—		
E_{ts}	Total Switching Loss	—	0.85	—		
L_E	Internal Emitter Inductance	—	7.5	—		
C_{ies}	Input Capacitance	—	1900	—	pF	See Fig. 7
C_{oes}	Output Capacitance	—	140	—		
C_{res}	Reverse Transfer Capacitance	—	35	—		

Notes:

- ① Repetitive rating; $V_{GE} = 20V$, pulse width limited by max. junction temperature. (See fig. 13b)
- ② $V_{CC} = 80\%(V_{CES})$, $V_{GE} = 20V$, $L = 10\mu H$, $R_G = 10\Omega$, (See fig. 13a)
- ③ Repetitive rating; pulse width limited by maximum junction temperature.
- ④ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ⑤ Pulse width $5.0\mu s$, single shot.

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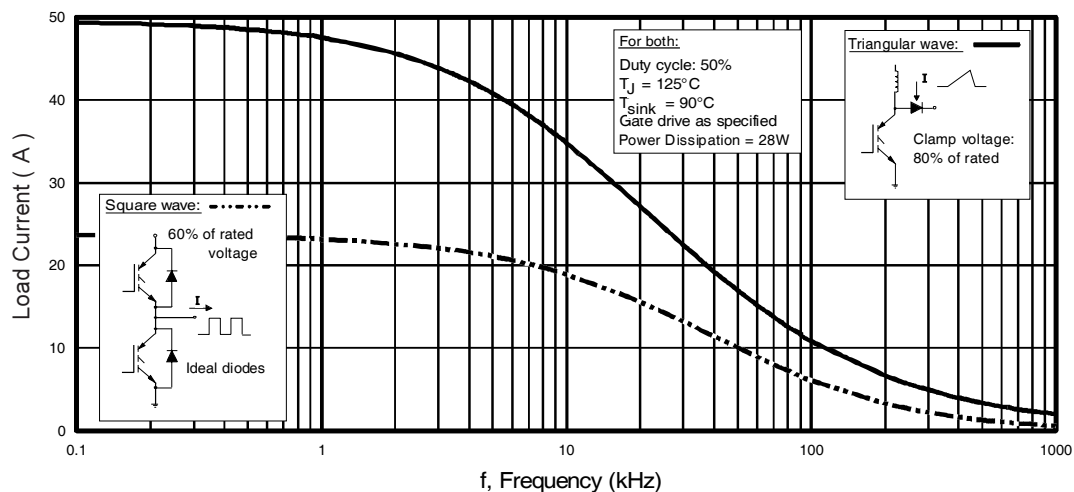


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

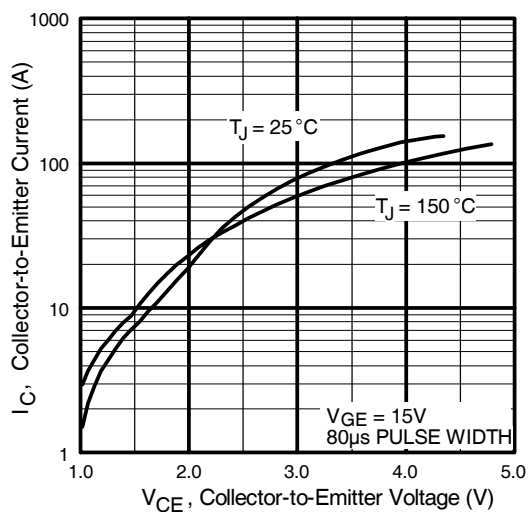


Fig. 2 - Typical Output Characteristics

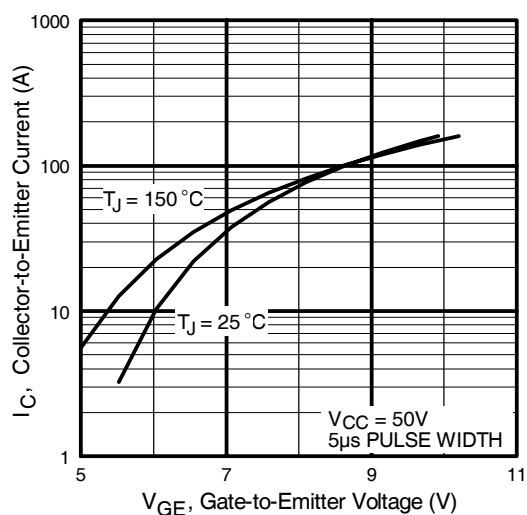


Fig. 3 - Typical Transfer Characteristics

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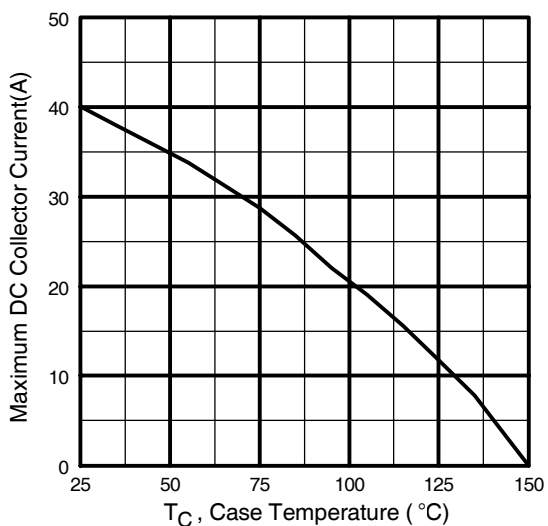


Fig. 4 - Maximum Collector Current vs. Case Temperature

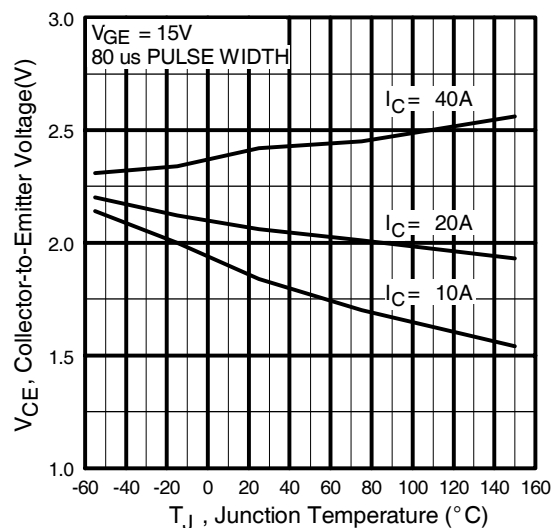


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

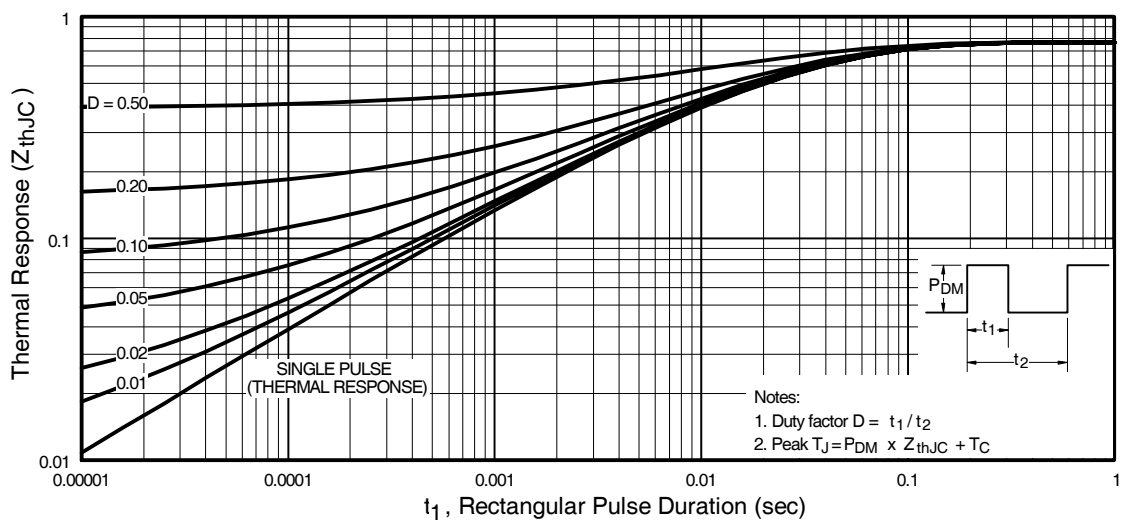


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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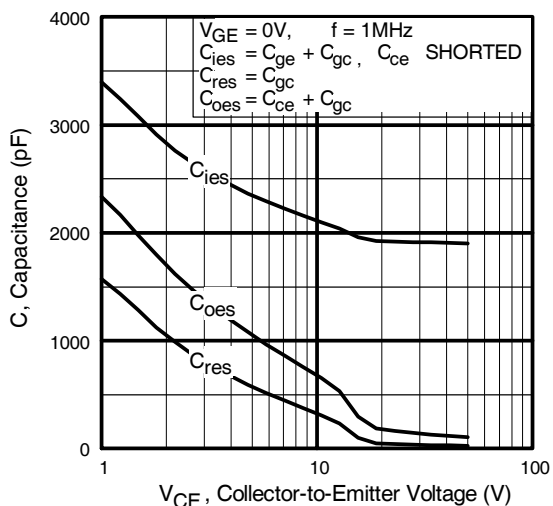


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

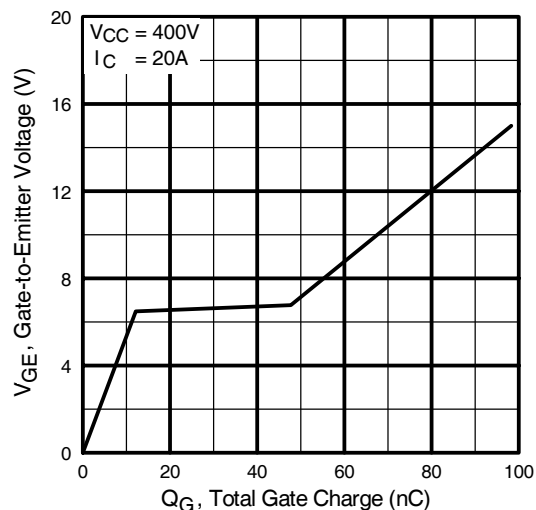


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

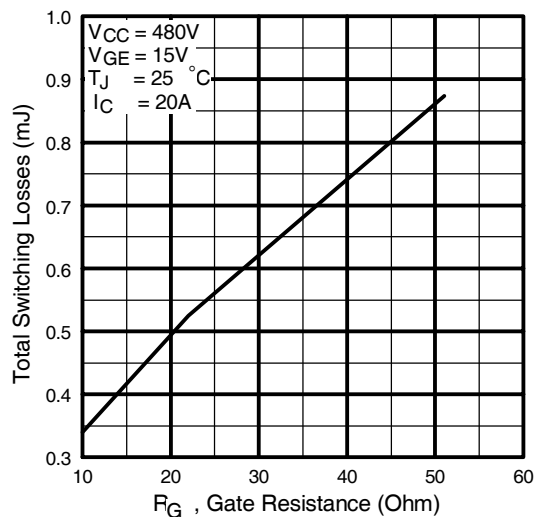


Fig. 9 - Typical Switching Losses vs. Gate Resistance

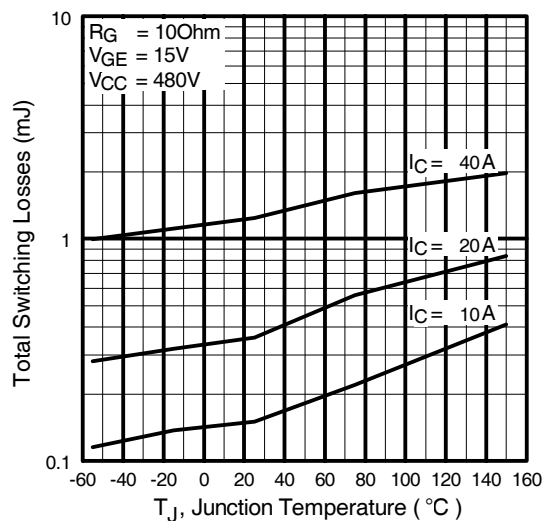


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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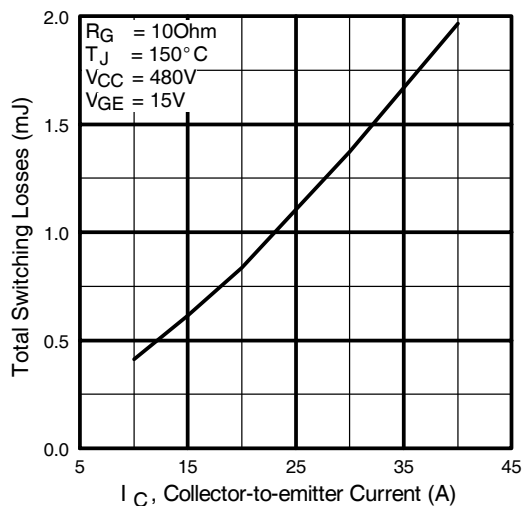


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

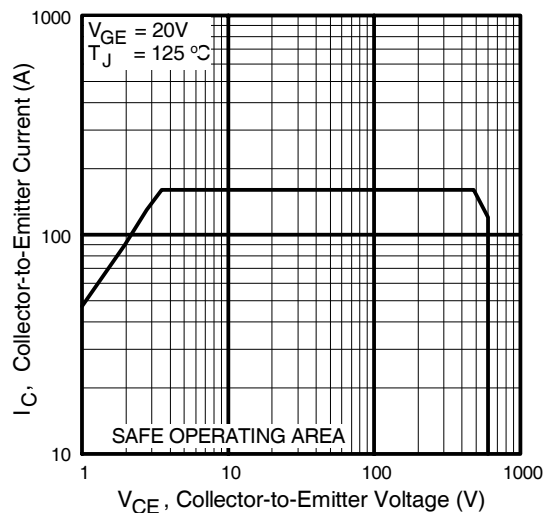
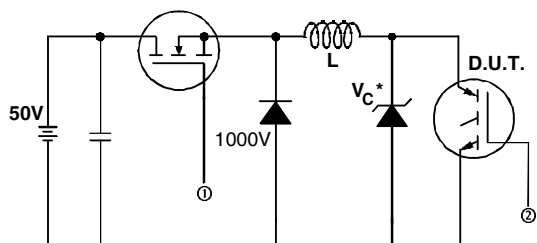


Fig. 12 - Turn-Off SOA

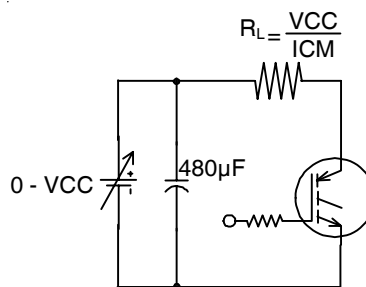
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* Driver same type as D.U.T.; $V_c = 80\%$ of $V_{ce(max)}$
* Note: Due to the 50V power supply, pulse width and inductor will increase to obtain rated I_d .

Fig. 13a - Clamped Inductive Load Test Circuit



Pulsed Collector Current Test Circuit

Fig. 13b - Pulsed Collector Current Test Circuit

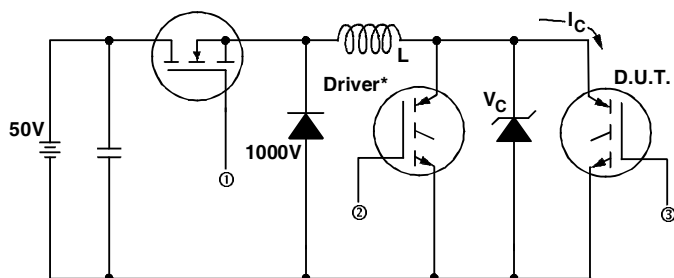


Fig. 14a - Switching Loss Test Circuit

* Driver same type as D.U.T., $V_c = 480V$

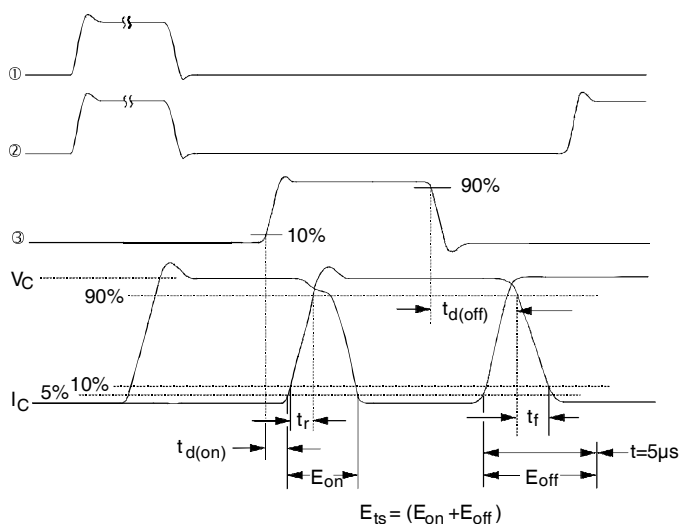


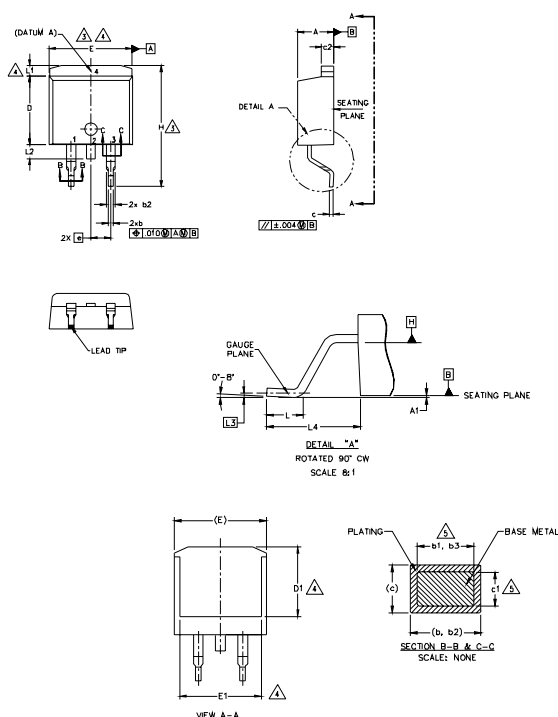
Fig. 14b - Switching Loss Waveforms

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)

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SYMBOL	DIMENSIONS				UNIT
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.066	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3, 4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.10	
L1	—	1.65	—	.066	4
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.13mm (0.005") PER SIDE. DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
 4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
 5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 7. CONTROLLING DIMENSION: INCH.
 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.- CATHODE
3.- ANODE

HEXEET

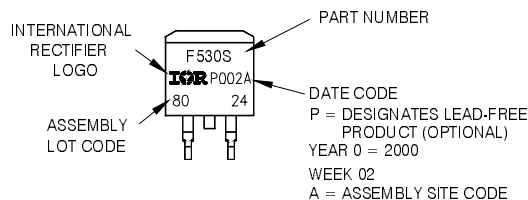
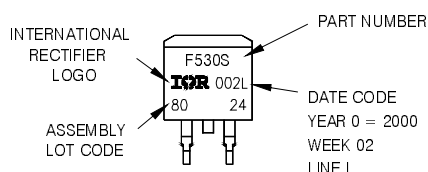
- | | |
|--------------|------------------|
| 1.- GATE | 1.- GATE |
| 2, 4.- DRAIN | 2, 4.- COLLECTOR |
| 3.- SOURCE | 3.- EMITTER |

D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE 'L'

Note: 'P' in assembly line position indicates 'Lead-Free'

OR



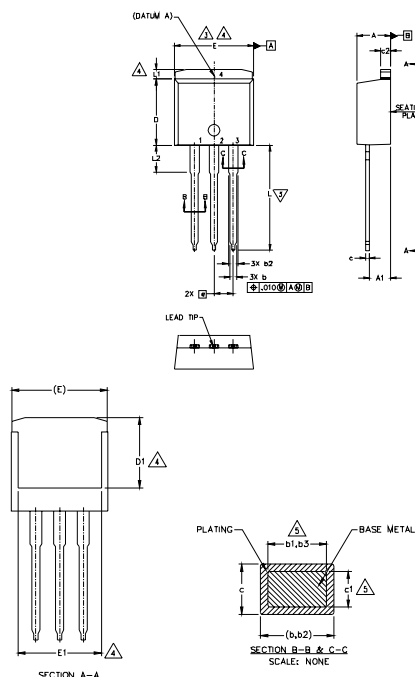
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/pkigbt.html>

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IRG4BC40WS/LPbF

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3, 4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	—	1.65	—	.065	4
L2	3.56	3.71	.140	.146	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .127 (.005") PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION D1 AND E1 APPLY TO BASE METAL ONLY.
5. INTERNAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORMS TO JEDEC TO-262 EXCEPT A1 (min.), b (min.), and D1 (min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IRG4BC40WS/LPbF

- 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

DIODES

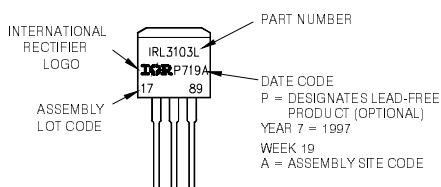
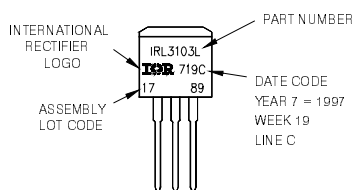
- 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN
- 1. ANODE (TWO DI) / OPEN (ONE DI)
- 2. 4. CATHODE
- 3. ANODE

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE 'C'

Note: 'P' in assembly line position indicates 'Lead-Free'

OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/pkight.html>

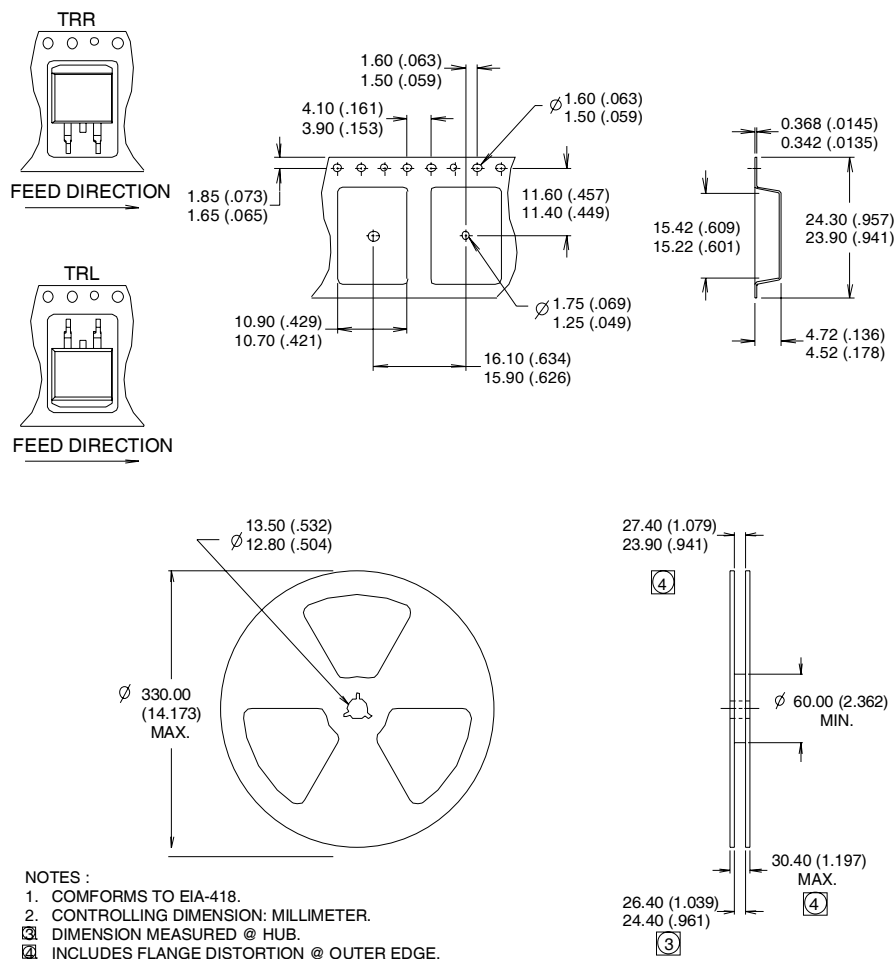
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D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/pkight.html>

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