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ON Semiconductor
MC100LVEP11DTG

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# MC10LVEP11, MC100LVEP11

# 2.5 V / 3.3 V ECL 1:2 Differential Fanout Buffer

## Description

The MC10/100LVEP11 is a differential 1:2 fanout buffer. The device is pin and functionally equivalent to the EP11 device. With AC performance the same as the EP11 device, the LVEP11 is ideal for applications requiring lower voltage. Single-ended CLK input operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in NECL mode.

The 100 Series contains temperature compensation.

## Features

- 240 ps Typical Propagation Delay
- Maximum Frequency > 3.0 GHz Typical
- PECL Mode Operating Range:
  - ♦ $V_{CC}$ = 2.375 V to 3.8 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  - ♦ $V_{CC}$ = 0 V with $V_{EE}$ = −2.375 V to −3.8 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at $V_{EE}$
- LVDS Input Compatible
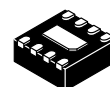- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

**ON Semiconductor®**
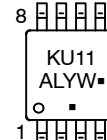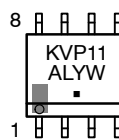
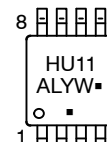**www.onsemi.com**



| SOIC−8 NB D SUFFIX CASE 751−07 | TSSOP−8 DT SUFFIX CASE 948R−02 | DFN−8 MN SUFFIX CASE 506AA |
| --- | --- | --- |

**MARKING DIAGRAMS\***



```
HVP11        HU11        5X M
ALYW         ALYW

KVP11        KU11        4K M
ALYW         ALYW
```
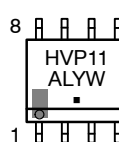
| H | = MC10 | A | = Assembly Location |
| --- | --- | --- | --- |
| K | = MC100 | L | = Wafer Lot |
| 5X | = MC10 | Y | = Year |
| 4K | = MC100 | W | = Work Week |
| | | $\overline{M}$ | = Date Code |
| | | ■ | = Pb-Free Package |

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

## ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.
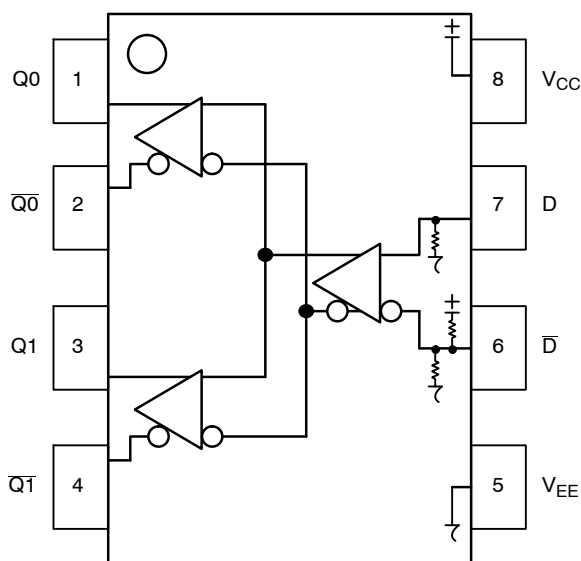
## MC10LVEP11, MC100LVEP11



**Figure 1. 8-Lead Pinout** (Top View) **and Logic Diagram**

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| D*, $\overline{D}$** | ECL Data Inputs |
| Q0, $\overline{Q0}$, Q1, $\overline{Q1}$ | ECL Data Outputs |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| EP | (DFN−8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

*Pins will default to 2/3 $V_{CC}$ when left open.
**Pins will default LOW when left open.

**Table 2. ATTRIBUTES**

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | 37.5 kΩ |
| ESD Protection<br>　　Human Body Model<br>　　Machine Model<br>　　Charged Device Model | > 4 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb-Free Pkg |
| 　SOIC−8 NB<br>　TSSOP−8<br>　DFN−8 | Level 1<br>Level 3<br>Level 1 |
| Flammability Rating<br>　　Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | 110 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1.  For additional information, see Application Note AND8003/D.

## MC10LVEP11, MC100LVEP11

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE} = 0$ V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC} = 0$ V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE} = 0$ V<br>$V_{CC} = 0$ V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>−6 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC−8 NB | 190<br>130 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC−8 NB | 41 to 44 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | TSSOP−8 | 185<br>140 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP−8 | 41 to 44 | °C/W |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | DFN−8 | 129<br>84 | °C/W |
| $T_{sol}$ | Wave Solder (Pb-Free) | <2 to 3 sec @ 260°C | | 265 | °C |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | (Note 1) | DFN−8 | 35 to 40 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

## MC10LVEP11, MC100LVEP11

### Table 4. 10LVEP DC CHARACTERISTICS, PECL ($V_{CC}$ = 2.5 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 25 | 33 | 40 | 29 | 33 | 40 | 32 | 34 | 42 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 1365 | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 565 | 740 | 865 | 630 | 805 | 930 | 690 | 865 | 990 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | µA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.125 V to −1.3 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Single-Ended input CLK pin operation is limited to $V_{CC} \geq$ 3.0 V in PECL mode.

### Table 5. 10LVEP DC CHARACTERISTICS, PECL ($V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 25 | 33 | 40 | 29 | 33 | 40 | 32 | 34 | 42 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 2165 | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 1365 | 1540 | 1665 | 1430 | 1605 | 1730 | 1490 | 1665 | 1790 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) (Note 3) | 2090 | | 2415 | 2155 | | 2480 | 2215 | | 2540 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) (Note 3) | 1365 | | 1690 | 1430 | | 1755 | 1490 | | 1815 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | µA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | µA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.925 V to −0.5 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. Single-Ended input CLK pin operation is limited to $V_{CC} \geq$ 3.0 V in PECL mode.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

## MC10LVEP11, MC100LVEP11

### Table 6. 10LVEP DC CHARACTERISTICS, NECL ($V_{CC}$ = 0 V, $V_{EE}$ = −3.8 V to −2.375 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 25 | 33 | 40 | 29 | 33 | 40 | 32 | 34 | 42 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1135 | −1010 | −885 | −1070 | −945 | −820 | −1010 | −885 | −760 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1935 | −1760 | −1635 | −1870 | −1695 | −1570 | −1810 | −1635 | −1510 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) (Note 3) | −1210 | | −885 | −1145 | | −820 | −1085 | | −760 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) (Note 3) | −1935 | | −1610 | −1870 | | −1545 | −1810 | | −1485 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current $\quad$D $\quad\overline{D}$ | 0.5 −150 | | | 0.5 −150 | | | 0.5 −150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. Single-Ended input CLK pin operation is limited to $V_{EE} \leq$ −3.0 V in NECL mode.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

### Table 7. 100LVEP DC CHARACTERISTICS, PECL ($V_{CC}$ = 2.5 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 25 | 35 | 42 | 29 | 38 | 46 | 32 | 41 | 50 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 555 | 730 | 900 | 555 | 730 | 900 | 555 | 730 | 900 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 1335 | | 1620 | 1335 | | 1620 | 1335 | | 1620 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 555 | | 900 | 555 | | 900 | 555 | | 900 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current $\quad$D $\quad\overline{D}$ | 0.5 −150 | | | 0.5 −150 | | | 0.5 −150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.125 V to −1.3 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Single-Ended input CLK pin operation is limited to $V_{CC} \geq$ 3.0 V in PECL mode.

## MC10LVEP11, MC100LVEP11

**Table 8. 100LVEP DC CHARACTERISTICS, PECL** ($V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 25 | 35 | 42 | 29 | 38 | 46 | 32 | 41 | 50 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 1355 | 1530 | 1700 | 1355 | 1530 | 1700 | 1355 | 1530 | 1700 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) (Note 3) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) (Note 3) | 1355 | | 1700 | 1355 | | 1700 | 1355 | | 1700 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.925 V to −0.5 V.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. Single-Ended input CLK pin operation is limited to $V_{CC} \geq 3.0$ V in PECL mode.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 9. 100LVEP DC CHARACTERISTICS, NECL** ($V_{CC}$ = 0 V; $V_{EE}$ = −3.8 V to −2.375 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 25 | 35 | 42 | 29 | 38 | 46 | 32 | 41 | 50 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1945 | −1770 | −1600 | −1945 | −1770 | −1600 | −1945 | −1770 | −1600 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) (Note 3) | −1165 | | −880 | −1165 | | −880 | −1165 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) (Note 3) | −1945 | −1425 | −1600 | −1945 | −1425 | −1600 | −1945 | −1425 | −1600 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | $V_{EE}$+1.2 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current<br>D<br>$\overline{D}$ | 0.5<br>−150 | | | 0.5<br>−150 | | | 0.5<br>−150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with $V_{CC}$.
2. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
3. Single-Ended input CLK pin operation is limited to $V_{EE} \leq −3.0$ V in NECL mode.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

## MC10LVEP11, MC100LVEP11

**Table 10. AC CHARACTERISTICS** ($V_{CC}$ = 0 V; $V_{EE}$ = −3.8 V to −2.375 V or $V_{CC}$ = 2.375 V to 3.8 V; $V_{EE}$ = 0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Maximum Frequency (Figure 2) | | 3 | | | 3 | | | 3 | | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay (Differential Configuration) CLK to Q, $\overline{Q}$ | 170 | 230 | 300 | 180 | 240 | 310 | 210 | 270 | 360 | ps |
| $t_{SKEW}$ | Within Device Skew        Q, $\overline{Q}$ Device to Device Skew (Note 2) | | 5.0 | 20 130 | | 5.0 | 20 130 | | 5.0 | 20 150 | ps |
| $t_{JITTER}$ | CLOCK Random Jitter (RMS) @ ≤1.0 GHz @ ≤1.5 GHz @ ≤2.0 GHz @ ≤2.5 GHz @ ≤3.0 GHz | | 0.126 0.112 0.111 0.112 0.155 | 0.3 0.2 0.3 0.2 0.2 | | 0.142 0.162 0.122 0.172 0.217 | 0.4 0.3 0.2 0.3 0.3 | | 0.209 0.162 0.170 0.235 0.368 | 0.3 0.2 0.3 0.3 0.6 | ps |
| $V_{PP}$ | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| $t_r$ $t_f$ | Output Rise/Fall Times     Q, $\overline{Q}$ (20% – 80%) | 70 | 110 | 170 | 80 | 120 | 180 | 100 | 140 | 200 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC}$ − 2.0 V.
2. Skew is measured between outputs under identical transitions.
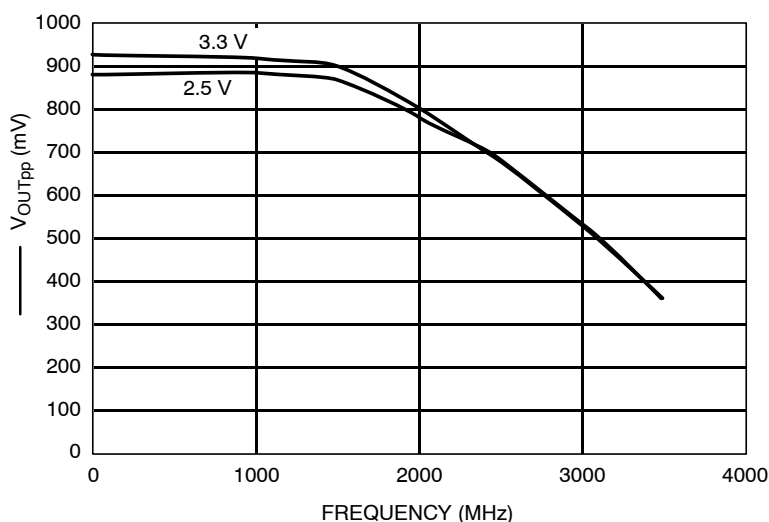


**Figure 2. $F_{max}$ Typical**

## MC10LVEP11, MC100LVEP11
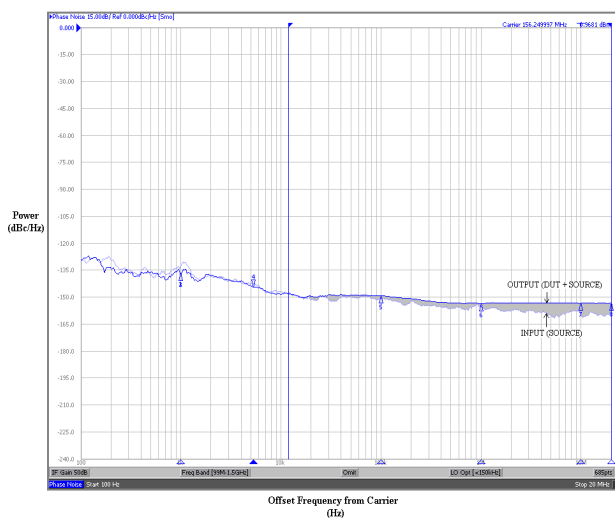


**Figure 3. Typical Phase Noise Plot at**
$f_{carrier}$ = 156.25 MHz
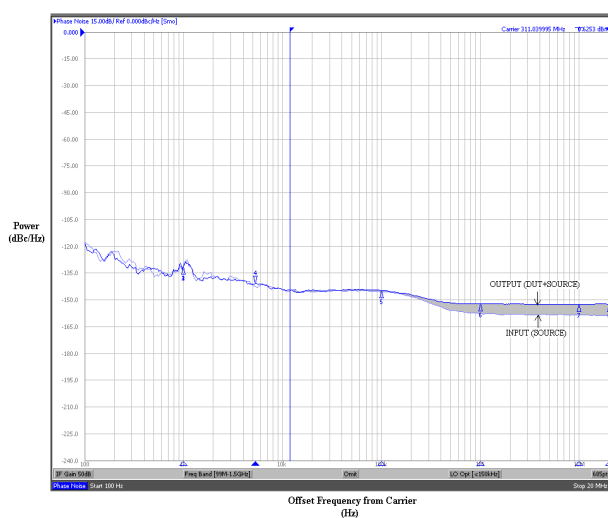


**Figure 4. Typical Phase Noise Plot at**
$f_{carrier}$ = 311.04 MHz
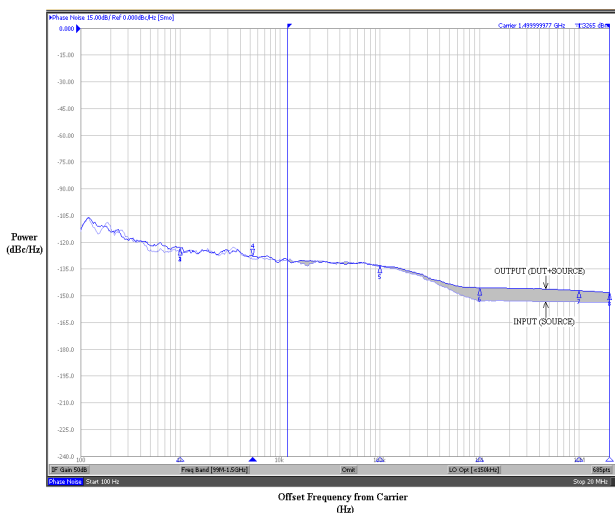


**Figure 5. Typical Phase Noise Plot at**
$f_{carrier}$ = 1.5 GHz
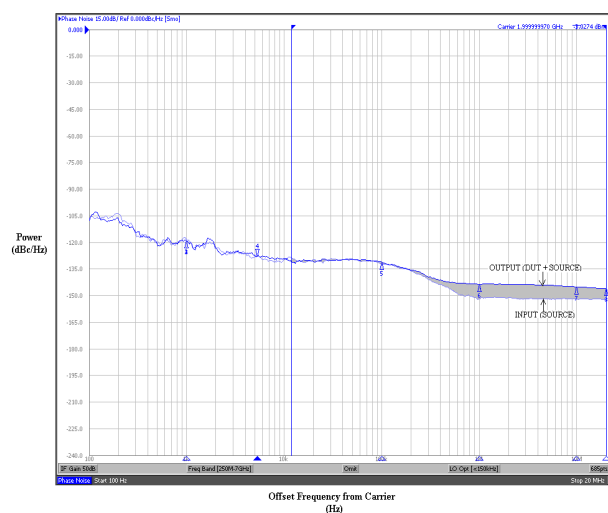


**Figure 6. Typical Phase Noise Plot at**
$f_{carrier}$ = 2 GHz

The above phase noise plots captured using Agilent E5052A show additive phase noise of the MC100LVEP11 device at frequencies 156.25 MHz, 311.04 MHz, 1.5 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 66 fs, 37 fs, 14 fs and 13 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

## MC10LVEP11, MC100LVEP11
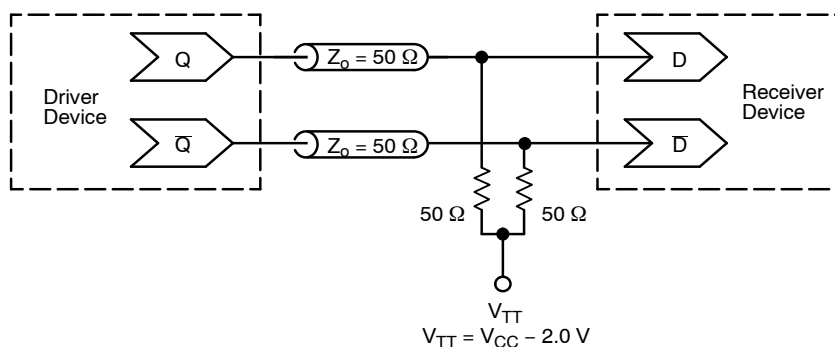


**Figure 7. Typical Termination for Output Driver and Device Evaluation**
**(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC10LVEP11DG | SOIC−8 NB (Pb-Free) | 98 Units / Rail |
| MC10LVEP11DR2G | SOIC−8 NB (Pb-Free) | 2500 / Tape & Reel |
| MC10LVEP11DTG | TSSOP−8 (Pb-Free) | 100 Units / Rail |
| MC10LVEP11DTR2G | TSSOP−8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LVEP11DG | SOIC−8 (Pb-Free) | 98 Units / Rail |
| MC100LVEP11DR2G | SOIC−8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LVEP11DTG | TSSOP−8 (Pb-Free) | 100 Units / Rail |
| MC100LVEP11DTR2G | TSSOP−8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LVEP11MNR4G | DFN−8 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MC10LVEP11, MC100LVEP11

**Resource Reference of Application Notes**

| | | |
|---|---|---|
| **AN1405**/D | – | ECL Clock Distribution Techniques |
| **AN1406**/D | – | Designing with PECL (ECL at +5.0 V) |
| **AN1503**/D | – | ECLinPS™ I/O SPiCE Modeling Kit |
| **AN1504**/D | – | Metastability and the ECLinPS Family |
| **AN1568**/D | – | Interfacing Between LVDS and ECL |
| **AN1672**/D | – | The ECL Translator Guide |
| **AND8001**/D | – | Odd Number Counters Design |
| **AND8002**/D | – | Marking and Date Codes |
| **AND8020**/D | – | Termination of ECL Logic Devices |
| **AND8066**/D | – | Interfacing with ECLinPS |
| **AND8090**/D | – | AC Characteristics of ECL Devices |

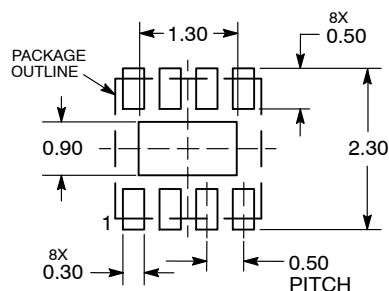## MC10LVEP11, MC100LVEP11

### PACKAGE DIMENSIONS

**SOIC−8 NB**
CASE 751−07
ISSUE AK
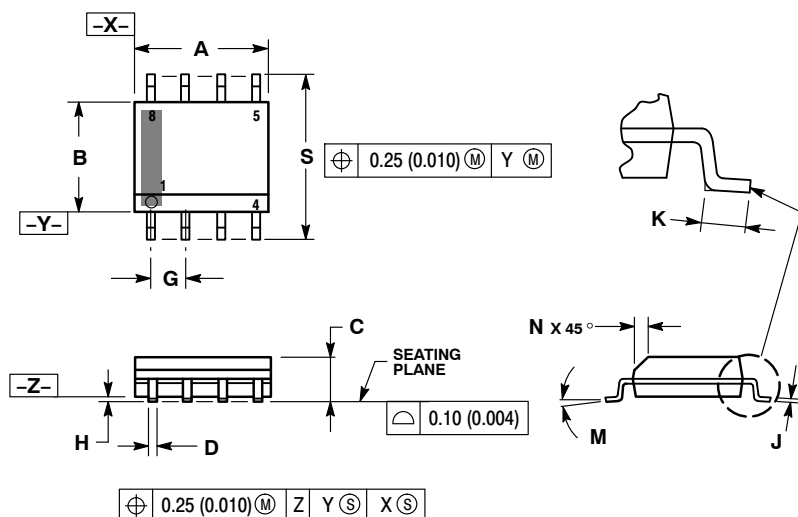
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|------|------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

### SOLDERING FOOTPRINT*
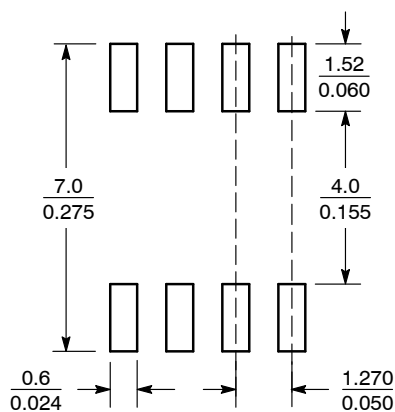
SCALE 6:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## MC10LVEP11, MC100LVEP11

### PACKAGE DIMENSIONS

**TSSOP−8**
CASE 948R−02
ISSUE A
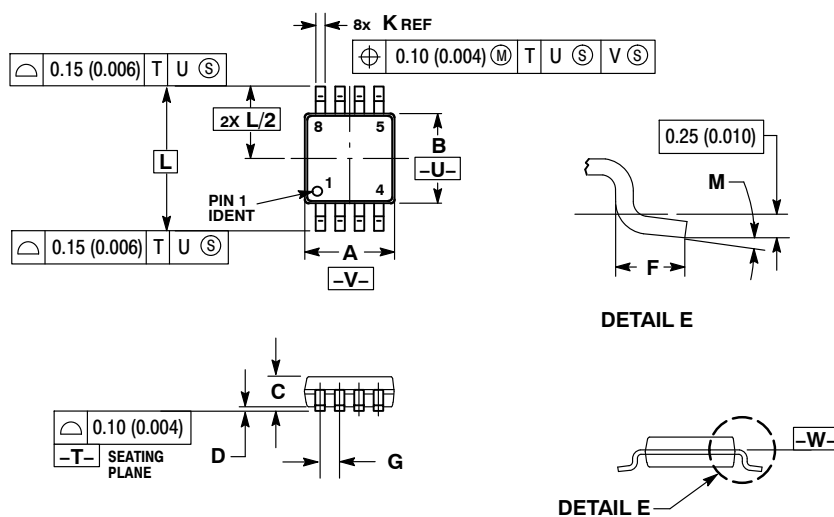


**DETAIL E**

**SEATING PLANE**

**DETAIL E**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.80 | 1.10 | 0.031 | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.40 | 0.70 | 0.016 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| K | 0.25 | 0.40 | 0.010 | 0.016 |
| L | 4.90 BSC | | 0.193 BSC | |
| M | 0° | 6° | 0° | 6° |

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electronic components

# MC10LVEP11, MC100LVEP11

## PACKAGE DIMENSIONS

**DFN−8 2x2, 0.5P**
CASE 506AA
ISSUE F
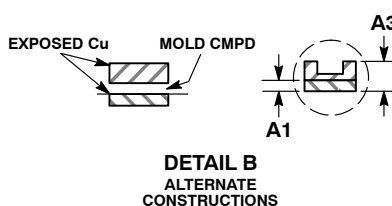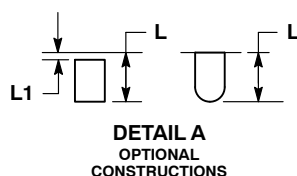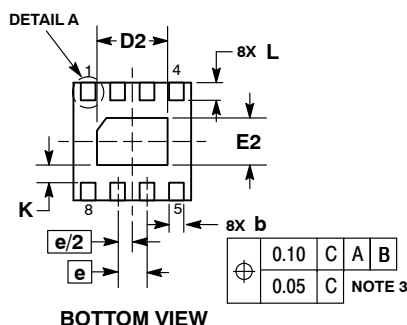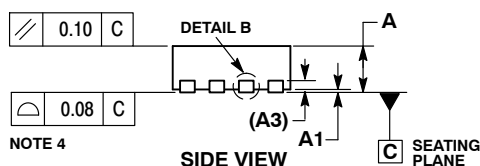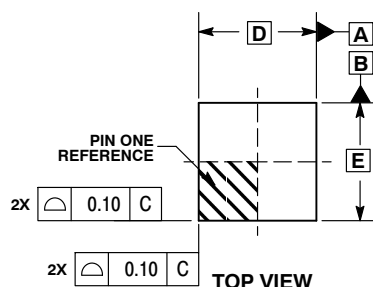
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**PIN ONE REFERENCE**

2X ⌓ 0.10 C

2X ⌓ 0.10 C

**TOP VIEW**

⌓ 0.10 C

⌓ 0.08 C
NOTE 4

**SIDE VIEW**

**DETAIL A**
OPTIONAL CONSTRUCTIONS

**DETAIL B**

EXPOSED Cu    MOLD CMPD

**DETAIL B**
ALTERNATE CONSTRUCTIONS

| DIM | MILLIMETERS | |
|-----|-----|-----|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.00 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.50 BSC | |
| K | 0.30 REF | |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |

**DETAIL A**

8X L

8X b

| ⊕ | 0.10 | C | A | B |
|---|------|---|---|---|
| | 0.05 | C | | NOTE 3 |

**BOTTOM VIEW**

## RECOMMENDED SOLDERING FOOTPRINT*

PACKAGE OUTLINE

8X 0.50

1.30

0.90

2.30

8X 0.30

0.50 PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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