N-Channel Power MOSFET 16A, 50V, 0.047 mΩ

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Features

- 16A, 50V

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFD16N05SM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	50	V
Drain to Gate Voltage (Note 1)	V_{DGR}	50	V
Continuous Drain Current	I_D	16	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Gate to Source Voltage	V_{GS}	±20	V
Pulsed Avalanche Rating	E_{AS}	Refer to Figure 5	
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NOTE

1. T_j

Elect

							NITS
Drain							V
Gate							V
Zero							µA
							µA
Gate							nA
Drain							Ω
Turn-							ns
Turn-							ns
Rise							ns
Turn-							ns
Fall T							ns
Turn-							ns
Total							nC
Gate							nC
Thres							nC
Input							pF
Outpu							pF
Reve							pF
Therr							C/W
Therr							C/W

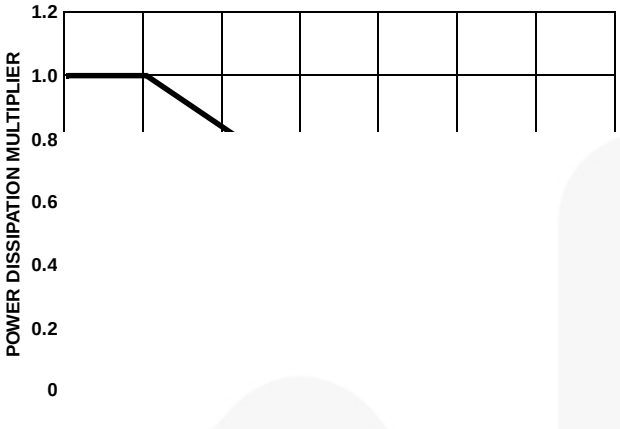
Sour

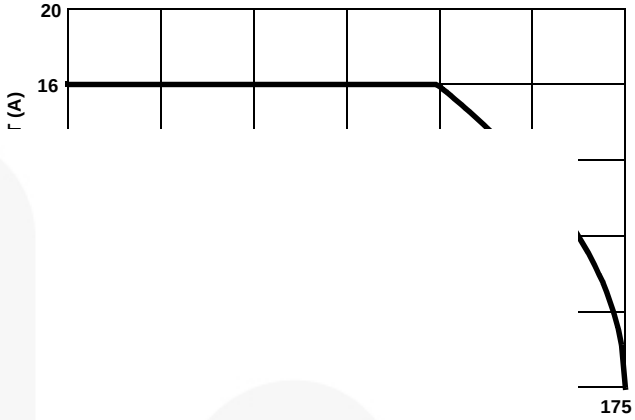
						NITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 16A	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 16A, dI_{SD}/dt = 100A/µs	-	-	125	ns

NOTES:

2. Pulse test: pulse width ≤250µs, duty cycle ≤2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified





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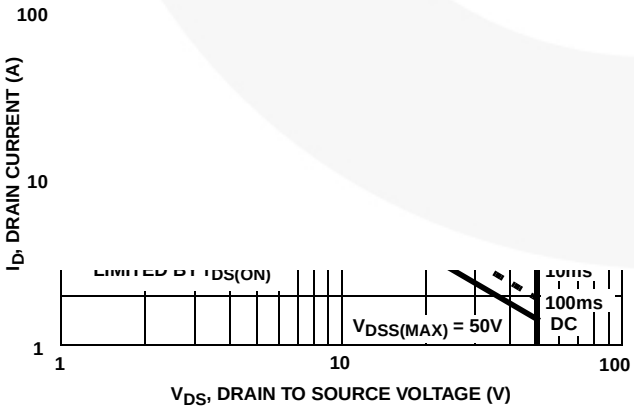


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

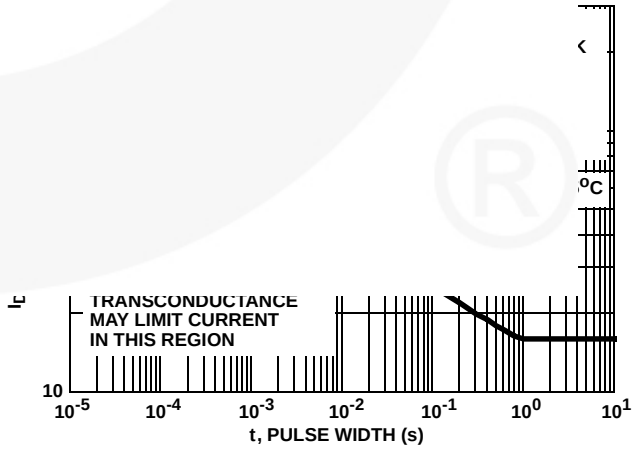
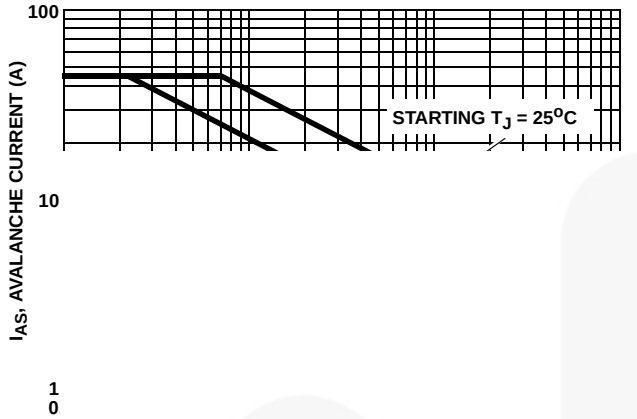
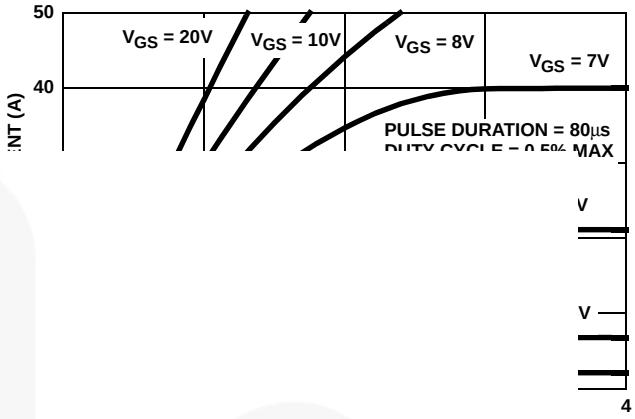


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified **(Continued)**





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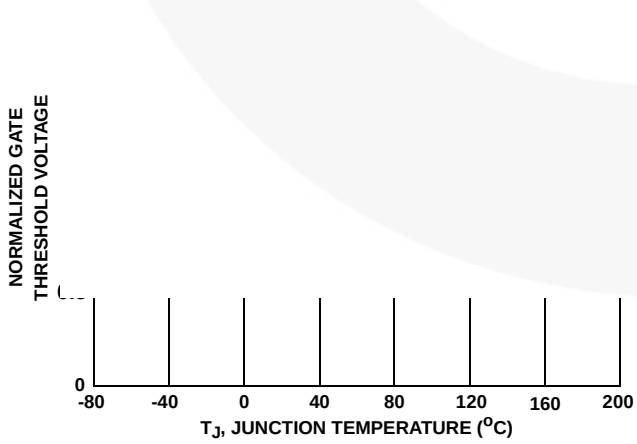


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

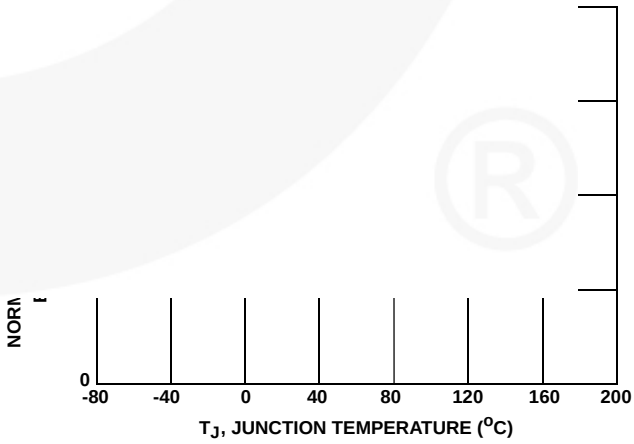
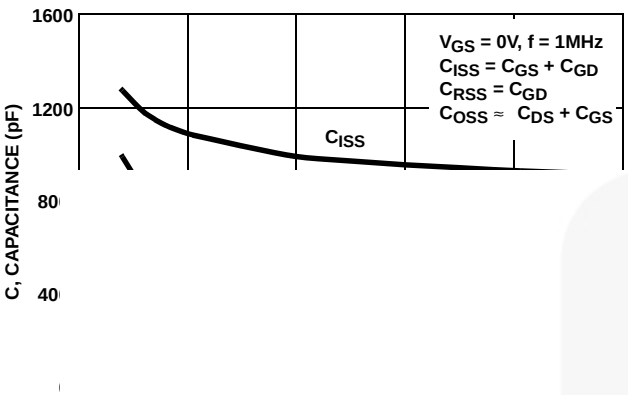
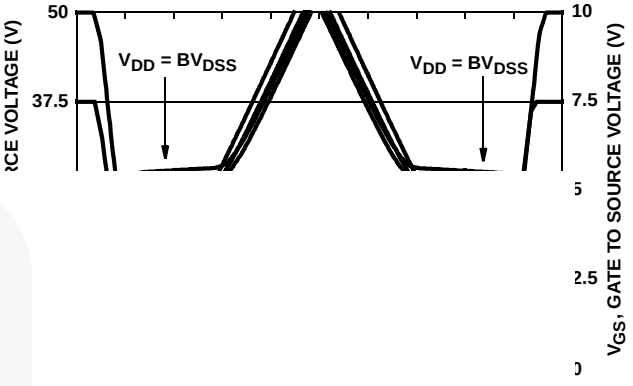


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**





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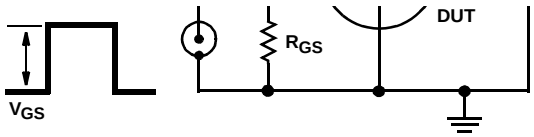


FIGURE 16. SWITCHING TIME TEST CIRCUIT

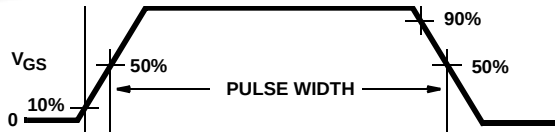
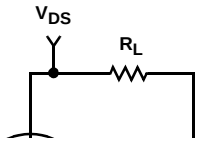
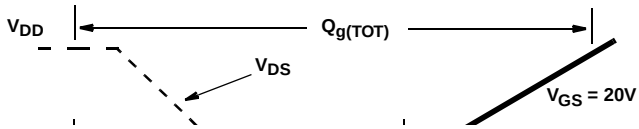


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

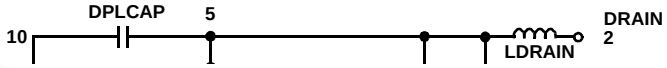




PSPICE Electrical Model

.SUBCKT RFD16N05 2 1 3 ; rev 10/31/94

CA 12 8 1.788e-10
CB 15 14 1.875e-10
CIN 6 8 8.33e-10



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NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

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