

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor](#)
[74VCXH16244MTD](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



November 1999
Revised June 2005

74VCXH16244

Low Voltage 16-Bit Buffer/Line Driver with Bushold

General Description

The VCXH16244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The VCXH16244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74VCXH16244 is designed for low voltage (1.2V to 3.6V) V_{CC} applications with output capability up to 3.6V.

The 74VCXH16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.2V to 3.6V V_{CC} supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminating the need for external pull-up/pull-down resistors
- t_{PD}
2.5 ns max for 3.0V to 3.6V V_{CC}
- Static Drive (I_{OH}/I_{OL})
 ± 24 mA @ 3.0V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
Human body model > 2000V
Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

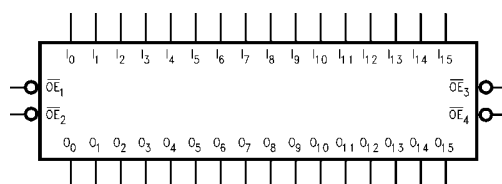
Ordering Code:

Order Number	Package Number	Package Description
74VCXH16244G (Note 1)(Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74VCXH16244MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: Ordering Code "G" indicates Tray.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

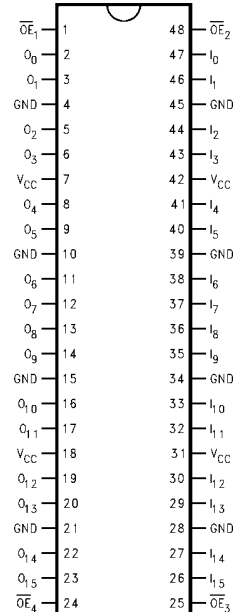


74VCXH16244 Low Voltage 16-Bit Buffer/Line Driver with Bushold

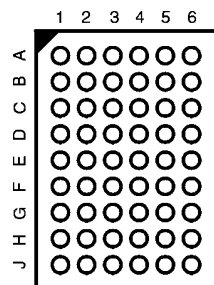
74VCXH16244

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0-I_{15}	Bushold Inputs
O_0-O_{15}	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O ₀	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	I ₀
B	O ₂	O ₁	NC	NC	I ₁	I ₂
C	O ₄	O ₃	V _{CC}	V _{CC}	I ₃	I ₄
D	O ₆	O ₅	GND	GND	I ₅	I ₆
E	O ₈	O ₇	GND	GND	I ₇	I ₈
F	O ₁₀	O ₉	GND	GND	I ₉	I ₁₀
G	O ₁₂	O ₁₁	V _{CC}	V _{CC}	I ₁₁	I ₁₂
H	O ₁₄	O ₁₃	NC	NC	I ₁₃	I ₁₄
J	O ₁₅	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	I ₁₅

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I ₀ -I ₃	O ₀ -O ₃
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I ₄ -I ₇	O ₄ -O ₇
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I ₈ -I ₁₁	O ₈ -O ₁₁
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I ₁₂ -I ₁₅	O ₁₂ -O ₁₅
L	L	L
L	H	H
H	X	Z

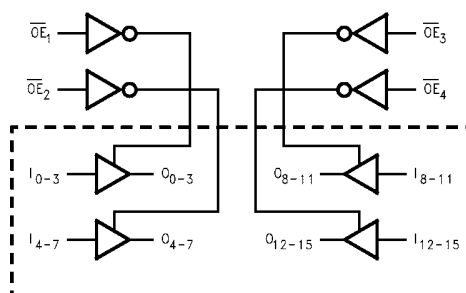
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Functional Description

The 74VCXH16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE out-

puts are controlled by an Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram



74VCXH16244

Absolute Maximum Ratings (Note 3)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 4)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 5)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0.0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	±24 mA
$V_{CC} = 2.3V$ to 2.7V	±18 mA
$V_{CC} = 1.65V$ to 2.3V	±6 mA
$V_{CC} = 1.4V$ to 1.6V	±2 mA
$V_{CC} = 1.2V$	±100 μA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6 1.2	2.0 1.6 0.65 x V_{CC} 0.65 x V_{CC} 0.65 x V_{CC}		V
V_{IL}	LOW Level Input Voltage		2.7 - 3.6 2.3 - 2.7 1.65 - 2.3 1.4 - 1.6 1.2		0.8 0.7 0.35 x V_{CC} 0.35 x V_{CC} 0.05 x V_{CC}	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	2.7 - 3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V
		$I_{OH} = -100 \mu A$ $I_{OH} = -6 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$	2.3 - 2.7 2.3 2.3 2.3	$V_{CC} - 0.2$ 2.0 1.8 1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6 \text{ mA}$	1.65 - 2.3 1.65	$V_{CC} - 0.2$ 1.25		
		$I_{OH} = -100 \mu A$ $I_{OH} = -2 \text{ mA}$	1.4 - 1.6 1.4	$V_{CC} - 0.2$ 1.05		
		$I_{OH} = -100 \mu A$	1.2	$V_{CC} - 0.2$		

DC Electrical Characteristics (Continued)						
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μ A	2.7 - 3.6		0.2	V
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 18 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
		I _{OL} = 100 μ A	2.3 - 2.7		0.2	
		I _{OL} = 12 mA	2.3		0.4	
		I _{OL} = 18 mA	2.3		0.6	
		I _{OL} = 100 μ A	1.65 - 2.3		0.2	
		I _{OL} = 6 mA	1.65		0.3	
		I _{OL} = 100 μ A	1.4 - 1.6		0.2	
		I _{OL} = 2 mA	1.4		0.35	
		I _{OL} = 100 μ A	1.2		0.05	
I _I	Input Leakage Current	Control Pins	0 $\leq$ V _I $\leq$ 3.6V	1.2 - 3.6	$\pm$ 5.0	μ A
		Data Pins	V _I = V _{CC} or GND	1.2 - 3.6	$\pm$ 5.0	μ A
I _{I(HOLD)}	Bushold Input Minimum Drive Hold Current	V _{IN} = 0.8V	3.0	75.0		μ A
		V _{IN} = 2.0V	3.0	-75.0		
		V _{IN} = 0.7V	2.3	45.0		
		V _{IN} = 1.6V	2.3	-45.0		
		V _{IN} = 0.57V	1.65	25.0		
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	(Note 6)	3.6	450		μ A
		(Note 7)	3.6	-450		
		(Note 6)	2.7	300		
		(Note 7)	2.7	-300		
		(Note 6)	1.95	200		
I _{OZ}	3-STATE Output Leakage	0 $\leq$ V _O $\leq$ 3.6V	2.7 - 3.6		$\pm$ 10.0	μ A
		V _I = V _{IH} or V _{IL}				
I _{OFF}	Power-OFF Leakage Current	0 $\leq$ (V _O) $\leq$ 3.6V	0		10.0	μ A
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.2 - 3.6		20.0	μ A
		V _{CC} $\leq$ (V _O) $\leq$ 3.6V (Note 8)	1.2 - 3.6		$\pm$ 20.0	μ A
Δ I _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		750	μ A
Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH. Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW. Note 8: Outputs disabled or 3-STATE only.						

74VCXH16244

AC Electrical Characteristics (Note 9)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units	Figure Number
				Min	Max		
t _{PHL} t _{PLH}	Propagation Delay	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	2.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.0		
			1.8 ± 0.15	1.5	6.0		
		C _L = 15 pF, R _L = 2 kΩ	1.5 ± 0.1	1.0	12.0	ns	Figures 5, 6
			1.2	1.5	30.0		
t _{PZL} t _{PZH}	Output Enable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.1		
			1.8 ± 0.15	1.5	8.2		
		C _L = 15 pF, R _L = 2 kΩ	1.5 ± 0.1	1.0	16.4	ns	Figures 5, 7, 8
			1.2	1.5	41.0		
t _{PLZ} t _{PHZ}	Output Disable Time	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	3.8		
			1.8 ± 0.15	1.5	6.8		
		C _L = 15 pF, R _L = 2 kΩ	1.5 ± 0.1	1.0	13.6	ns	Figures 5, 7, 8
			1.2	1.5	34.0		
t _{OSHL} t _{OSLH}	Output to Output Skew (Note 10)	C _L = 30 pF, R _L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C _L = 15 pF, R _L = 2 kΩ	1.5 ± 0.1		1.5	ns	
			1.2		1.5		

Note 9: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

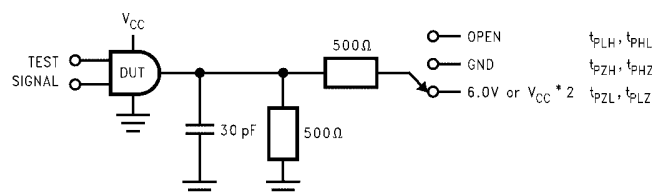
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V _{OHV}	Quiet Output Dynamic Valley V _{OH}	C _L = 30 pF, V _{IH} = V _{CC} , V _{IL} = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	T _A = +25°C	Units
			Typical	
C _{IN}	Input Capacitance	V _{CC} = 1.8, 2.5V or 3.3V, V _I = 0V or V _{CC}	6.0	pF
C _{OUT}	Output Capacitance	V _I = 0V or V _{CC} , V _{CC} = 1.8V, 2.5V or 3.3V	7.0	pF
C _{PD}	Power Dissipation Capacitance	V _I = 0V or V _{CC} , f = 10 MHz, V _{CC} = 1.8V, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms (V_{CC} 3.3V $\pm$ 0.3V to 1.8V $\pm$ 0.15V)



TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$; $1.8V \pm 0.15V$
t_{PZH} , t_{PHZ}	GND

FIGURE 1. AC Test Circuit

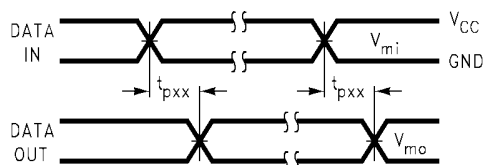


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

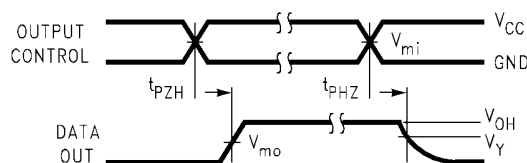


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

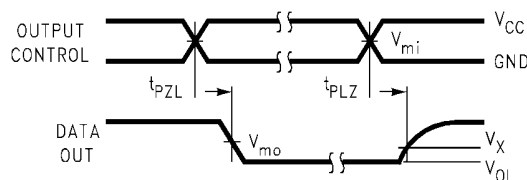


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

74VCXH16244

AC Loading and Waveforms ($V_{CC} 1.5 \pm 0.1V$ to $1.2V$)

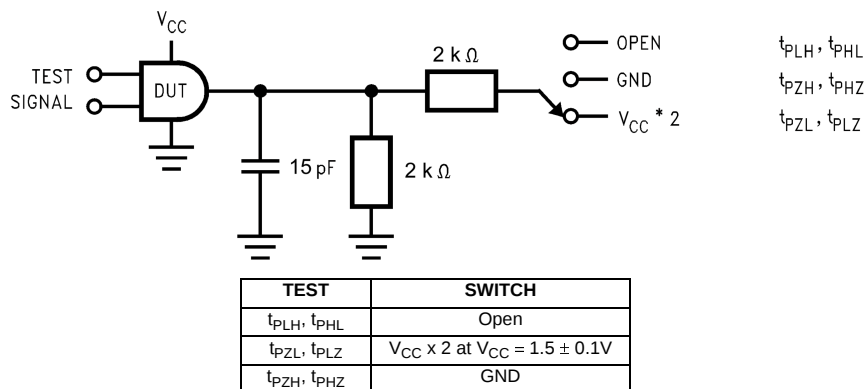


FIGURE 5. AC Test Circuit

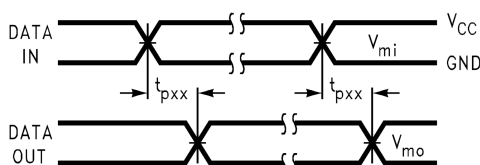


FIGURE 6. Waveform for Inverting and Non-Inverting Functions

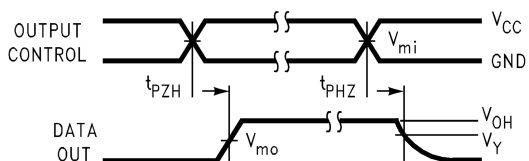


FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

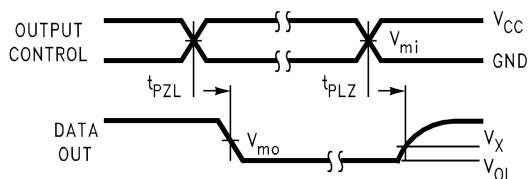
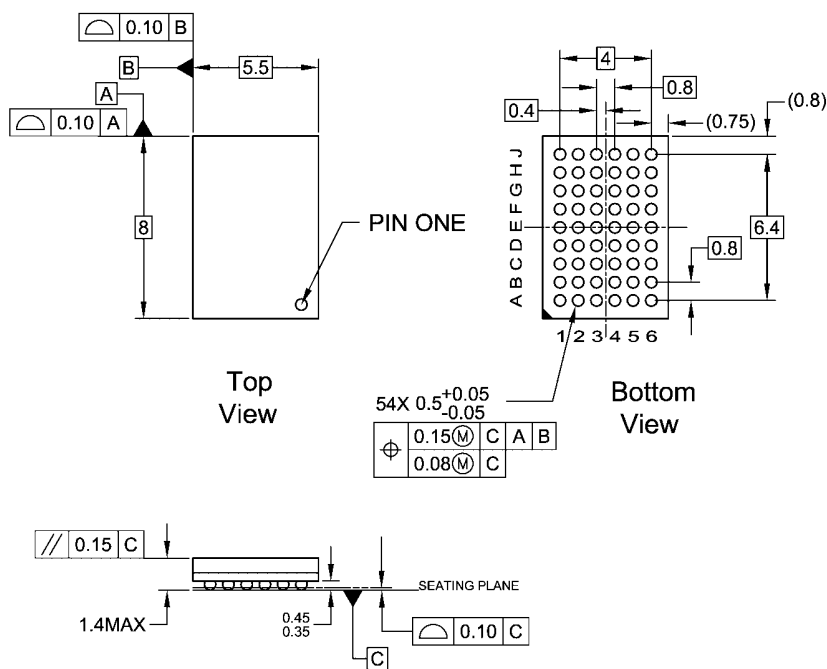


FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}
	$1.5V \pm 0.1V$
V_{mi}	$V_{CC}/2$
V_{mo}	$V_{CC}/2$
V_x	$V_{OL} + 0.1V$
V_y	$V_{OH} - 0.1V$

Physical Dimensions inches (millimeters) unless otherwise noted

NOTES:

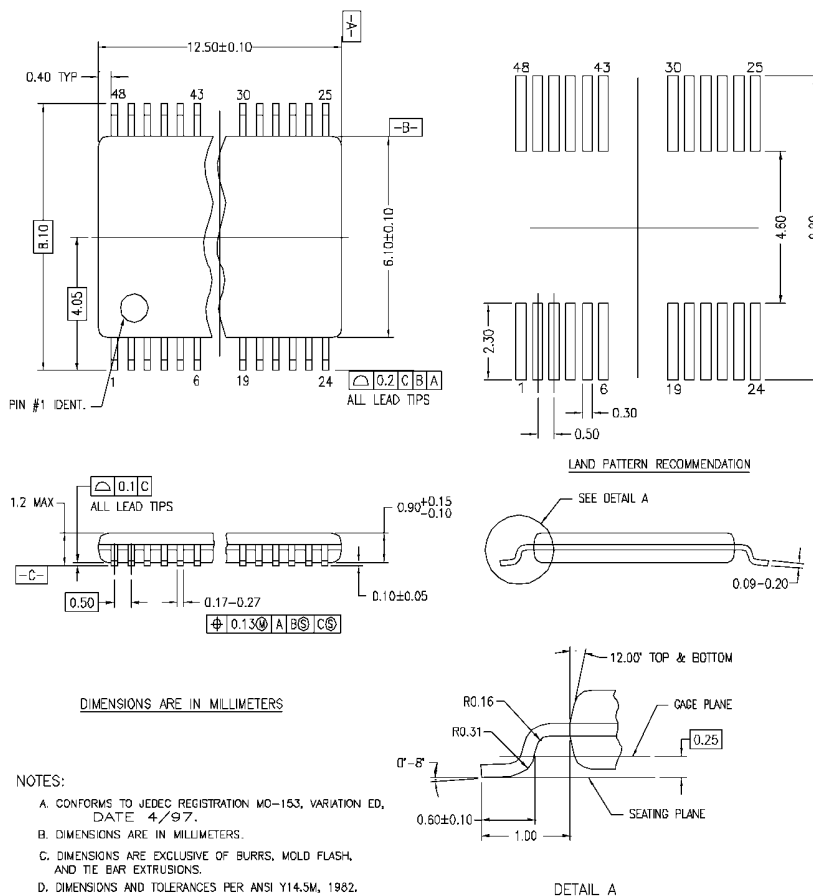
- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary**

74VCSX16244

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTD48REVC

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com