

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor](#)
[74ACTQ823SCX](#)

For any questions, you can email us directly:
sales@integrated-circuit.com



May 1991
 Revised September 2000

74ACTQ823 Quiet Series™ 9-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

The ACTQ823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The ACTQ823 utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

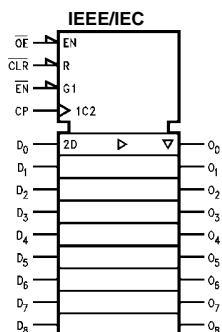
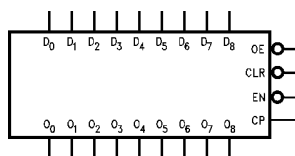
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- TTL compatible inputs

Ordering Code:

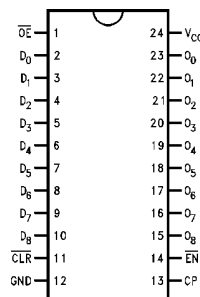
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74ACTQ823SC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74ACTQ823SPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering form.

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|--------------------------------|---------------|
| D ₀ -D ₈ | Data Inputs |
| O ₀ -O ₈ | Data Outputs |
| \overline{OE} | Output Enable |
| \overline{CLR} | Clear |
| CP | Clock Input |
| EN | Clock Enable |

FACT™, Quiet Series™, FACT Quiet Series™ and GTO™ are trademarks of Fairchild Semiconductor Corporation.

74ACTQ823

Functional Description

The ACTQ823 consists of nine D-type edge-triggered flip-flops. These have 3-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE} LOW, the contents of the flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops. In addition to the Clock and Output

Enable pins, there are Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins. These devices are ideal for parity bus interfacing in high performance systems.

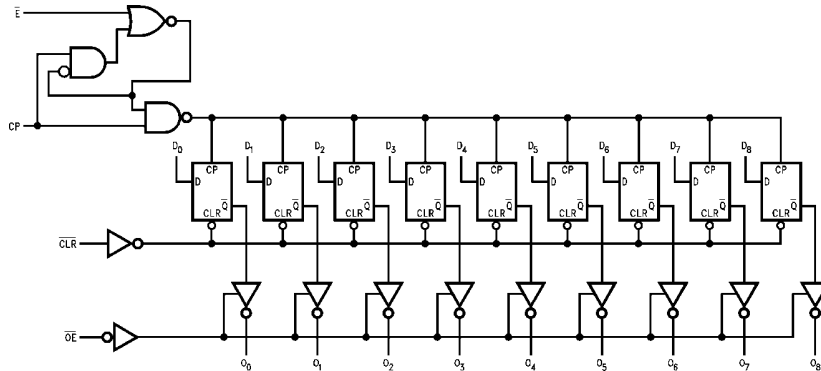
When \overline{CLR} is LOW and \overline{OE} is LOW, the outputs are LOW. When \overline{CLR} is HIGH, data can be entered into the flip-flops. When \overline{EN} is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the \overline{EN} is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

| Inputs | | | | | Internal | Output | Function |
|-----------------|------------------|-----------------|----|---|----------|--------|----------|
| \overline{OE} | \overline{CLR} | \overline{EN} | CP | D | | | |
| H | X | L | ↔ | L | L | Z | High Z |
| H | X | L | ↔ | H | H | Z | High Z |
| H | L | X | X | X | L | Z | Clear |
| L | L | X | X | X | L | L | Clear |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | Hold |
| H | H | L | ↔ | L | L | Z | Load |
| H | H | L | ↔ | H | H | Z | Load |
| L | H | L | ↔ | L | L | L | Load |
| L | H | L | ↔ | H | H | H | Load |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 ↔ = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| Absolute Maximum Ratings (Note 1) | | Recommended Operating Conditions | |
|--|--------------------------|---|----------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V | Supply Voltage (V_{CC}) | 4.5V to 5.5V |
| DC Input Diode Current (I_{IK}) | | Input Voltage (V_I) | 0V to V_{CC} |
| $V_I = -0.5V$ | -20 mA | Output Voltage (V_O) | 0V to V_{CC} |
| $V_I = V_{CC} + 0.5V$ | +20 mA | Operating Temperature (T_A) | -40°C to +85°C |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ | Minimum Input Edge Rate $\Delta V/\Delta t$ | 125 mV/ns |
| DC Output Diode Current (I_{OK}) | | V_{IN} from 0.8V to 2.0V | |
| $V_O = -0.5V$ | -20 mA | V_{CC} @ 4.5V, 5.5V | |
| $V_O = V_{CC} + 0.5V$ | +20 mA | | |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ | | |
| DC Output Source | | | |
| or Sink Current (I_O) | ± 50 mA | | |
| DC V_{CC} or Ground Current | | | |
| per Output Pin (I_{CC} or I_{GND}) | ± 50 mA | | |
| Storage Temperature (T_{STG}) | -65°C to +150°C | | |
| DC Latch-Up Source | | | |
| or Sink Current | ± 300 mA | | |
| Junction Temperature (T_J) | | | |
| PDIP | 140°C | | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for ACTQ

| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ C$ | | $T_A = -40^\circ C$ to $+85^\circ C$ | | Units | Conditions |
|-----------|--|-----------------|---------------------|-------------------|--------------------------------------|---------|--|------------|
| | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V_{OH} | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50 \mu A$ | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2) | |
| | | 5.5 | | 4.86 | 4.76 | | | |
| V_{OL} | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2) | |
| | | 5.5 | | 0.36 | 0.44 | | | |
| I_{IN} | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I = V_{CC}$, GND | |
| I_{OZ} | Maximum 3-STATE Leakage Current | 5.5 | | ± 0.5 | ± 5.0 | μA | $V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND | |
| I_{CCT} | Maximum I_{CC} /Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I_{OLD} | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max | |
| I_{OHD} | Output Current (Note 3) | 5.5 | | | -75 | mA | $V_{OHD} = 3.85V$ Min | |
| I_{CC} | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80.0 | μA | $V_{IN} = V_{CC}$ or GND | |
| V_{OLP} | Quiet Output Maximum Dynamic V_{OL} | 5.0 | 1.1 | 1.5 | | V | Figure 1, Figure 2 (Note 4)(Note 5) | |
| V_{OLV} | Quiet Output Minimum Dynamic V_{OL} | 5.0 | -0.6 | -1.2 | | V | Figure 1, Figure 2 (Note 4)(Note 5) | |
| V_{IHD} | Minimum HIGH Level Dynamic Input Voltage | 5.0 | 1.9 | 2.2 | | V | (Note 4)(Note 6) | |

74ACTQ823

| DC Electrical Characteristics for ACTQ (Continued) | | | | | | | | |
|--|--|------------------------------------|--|------------------------|---|---|-------|------------------|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -40°C to +85°C | | Units | Conditions |
| | | | Typ | Guaranteed Limits | | | | |
| V _{ILD} | Maximum LOW Level Dynamic Input Voltage | 5.0 | 1.2 | 0.8 | | | V | (Note 4)(Note 6) |
| <p>Note 2: All outputs loaded; thresholds on input associated with output under test.</p> <p>Note 3: Maximum test duration 2.0 ms, one output loaded at a time.</p> <p>Note 4: PDIP package.</p> <p>Note 5: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.</p> <p>Note 6: Max number of data inputs (n) switching. (n - 1) inputs switching 0V to 3V Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.</p> | | | | | | | | |
| AC Electrical Characteristics | | | | | | | | |
| Symbol | Parameter | V _{CC} (V) (Note 7) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} t _{PHL} | Propagation Delay CP to O _n | 5.0 | 2.0 | 7.0 | 9.0 | 2.0 | 10.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay CLR to O _n | 5.0 | 2.0 | 7.0 | 9.0 | 2.0 | 10.0 | ns |
| t _{PZH} t _{PZL} | Output Enable Time OE to O _n | 5.0 | 2.5 | 8.0 | 10.0 | 2.5 | 11.0 | ns |
| t _{PHZ} t _{PLZ} | Output Disable Time OE to O _n | 5.0 | 1.0 | 6.0 | 8.0 | 1.0 | 9.0 | ns |
| t _{OSLH} t _{OSHL} | Output to Output Skew D _n to O _n (Note 8) | 5.0 | | 0.5 | 1.0 | | 1.0 | ns |
| <p>Note 7: Voltage Range 5.0 is 5.0V ± 0.5V.</p> <p>Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.</p> | | | | | | | | |
| AC Operating Requirements | | | | | | | | |
| Symbol | Parameter | V _{CC} (V) (Note 9) | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | |
| | | | Typ | Guaranteed Minimum | | | | |
| t _S | Setup Time, HIGH or LOW D to CP | 5.0 | 0.5 | 3.0 | 3.0 | | ns | |
| t _H | Hold Time, HIGH or LOW D _n to CP | 5.0 | 0 | 1.5 | 1.5 | | ns | |
| t _S | Setup Time, HIGH or LOW EN to CP | 5.0 | 0 | 3.0 | 3.0 | | ns | |
| t _H | Hold Time, HIGH or LOW EN to CP | 5.0 | 0 | 1.5 | 1.5 | | ns | |
| t _W | CP Pulse Width, HIGH or LOW | 5.0 | 2.5 | 4.0 | 4.0 | | ns | |
| t _W | CLR Pulse Width, LOW | 5.0 | 3.0 | 4.0 | | | ns | |
| t _{REC} | CLR to CP Recovery Time | 5.0 | 1.5 | 3.5 | 4.0 | | ns | |
| <p>Note 9: Voltage Range 5.0 is 5.0V ± 0.5V</p> | | | | | | | | |
| Capacitance | | | | | | | | |
| Symbol | Parameter | Typ | Units | Conditions | | | | |
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = OPEN | | | | |
| C _{PD} | Power Dissipation Capacitance | 54 | pF | V _{CC} = 5.0V | | | | |

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

- Hewlett Packard Model 8180A Word Generator
- PC-163A Test Fixture
- Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.

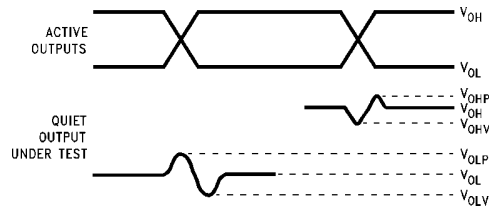


FIGURE 1. Quiet Output Noise Voltage Waveforms

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case transition for active and enable.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

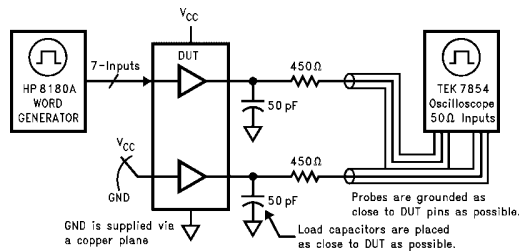
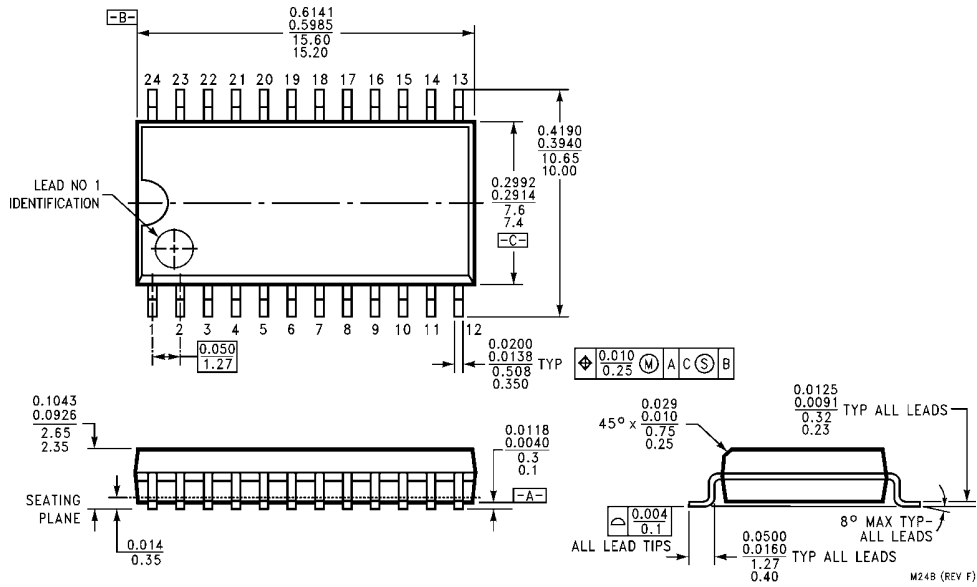


FIGURE 2. Simultaneous Switching Test Circuit

74ACTQ823

Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
 Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C

N24C (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com