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Fairchild Semiconductor DM74AS873NT

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December 1986 Revised July 2003

DM74AS873

Dual 4-Bit D-Type Transparent Latches with 3-STATE Outputs

General Description

These dual 4-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM74AS873 are transparent D-type latches meaning that while the enable (G) is HIGH the Q outputs will follow the data (D) inputs. When the enable is taken LOW the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all outputs are on the other side.

Features

- Switching specifications at 50 pF
- \blacksquare Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly
- Space Saving 300 Mil Wide Package
- Bus structured pinout

Ordering Code:

Order Number	Package Number		Package [Description	
DM74AS873NT	N24C	24-Lead Plastic Dual-I	n-Line Package (PD	IP), JEDEC MS-001, 0.300" Wide	
Devices also available Connectio		by appending the suffix letter	"X" to the ordering code.		
EN	NABLE 1G 1Q1 1Q2	1Q3 1Q4 20 19	2Q1 2Q2 18 17	203 204 2G 2CLR 16 15 14 13	
-	G Q CLR D OC CLR D OC LR D OC	5 6 1D3 1D4	\$\bar{G} \ Q \ CLR \ D \ OC \ D \	9 10 11 12 2D3 2D4 20C GND	

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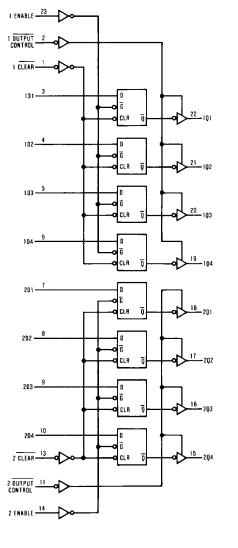
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Function Table

	Output			
CLR	D	EN	OC	Q
X	Х	Χ	Н	Z
L	Х	Χ	L	L
Н	Н	Н	L	Н
Н	L	Н	L	L
Н	Х	L	L	Q_0

- L = LOW State
 H = HIGH State
 X = Don't Care
 Z = High Impedance State
 Q₀ = Previous Condition of Q

Logic Diagram





Absolute Maximum Ratings(Note 1)

Supply Voltage 7V Input Voltage 7V Voltage Applied to Disabled Output 5.5V Operating Free Air Temperature Range $0^{\circ}\text{C to } +70^{\circ}\text{C}$

Storage Temperature Range -65°C to $+150^{\circ}\text{C}$

Typical θ_{JA}

N Package 47.0°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V _{CC}	Supply Voltage		4.5	5	5.5	V
V _{IH}	HIGH Level Input Voltage		2			V
V _{IL}	LOW Level Input Voltage				0.8	V
I _{OH}	HIGH Level Output Current				-15	mA
I _{OL}	LOW Level Output Current				48	mA
t _W	Pulse Width	Enable HIGH	5.5			
		Clear LOW	3.5			ns
t _{SU}	Data Setup Time (Note 2)		2↓			ns
t _H	Data Hold Time (Note 2)		3↓			ns
T _A	Free Air Operating Temperature		0		70	°C

Note 2: The (\$\psi\$) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Symbol	Parameter	Conditio	ns	Min	Тур	Max	Units
V _{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18 \text{ mA}$				-1.2	V
V _{OH}	HIGH Level	$V_{CC} = 4.5V$, $V_{IL} = Max$		2.4	3.3		V
	Output Voltage	I _{OH} = Max		2.4	3.3		v
		$I_{OH} = -2 \text{ mA}, V_{CC} = 4.5 \text{V to 5}$.5V	V _{CC} –2			V
V _{OL}	LOW Level	$V_{CC} = 4.5V, V_{IH} = 2V$			0.35	0.5	V
	Output Voltage	I _{OL} = Max			0.55	0.5	v
II	Input Current at Max	$V_{CC} = 5.5V, V_{IH} = 7V$				0.1	mA
	Input Voltage					0.1	IIIA
I _{IH}	HIGH Level Input Current	$V_{CC} = 5.5V, V_{IH} = 2.7V$				20	μΑ
I _{IL}	LOW Level Input Current	$V_{CC} = 5.5V, V_{IL} = 0.4V$				-0.5	mA
I _O (Note 3)	Output Drive Current	$V_{CC} = 5.5V, V_{O} = 2.25V$		-30		-112	mA
I _{OZH}	OFF-State Output Current,	$V_{CC} = 5.5V, V_{IH} = 2V$				50	μА
	HIGH Level Voltage Applied	$V_0 = 2.7V$				30	μΑ
I _{OZL}	OFF-State Output Current,	utput Current, V _{CC} = 5.5V, V _{IH} = 2V			-50	μА	
	LOW Level Voltage Applied	$V_0 = 0.4V$				-30	μΑ
I _{CC}	Supply Current	V _{CC} = 5.5V	Outputs HIGH		68	110	mA
		Outputs Open	Outputs LOW		67	109	mA
			Outputs Disabled		80	129	mA

Note 3: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit current, I_{OS}.



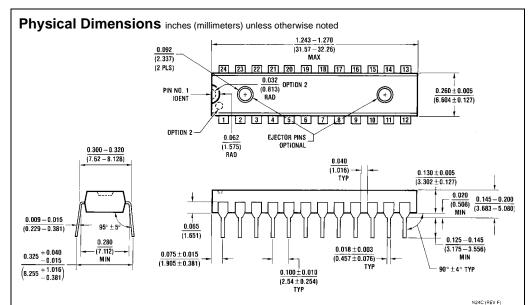
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Symbol	Parameter	Conditions	From	То	Min	Max	Units
t _{PLH}	Propagation Delay Time	V _{CC} = 4.5V to 5.5V	Data	Any Q	3	6.5	ns
	LOW-to-HIGH Level Output	$R_L = 500\Omega$		7 tily Q		0.0	
t _{PHL}	Propagation Delay Time	C _L = 50 pF	Data	Any Q	3	6	ns
	HIGH-to-LOW Level Output		Bala	Ally Q	3	· ·	110
t _{PLH}	Propagation Delay Time		Enable	Any Q	6	11.5	ns
	LOW-to-HIGH Level Output		Enable	7 tily Q		11.0	110
t _{PHL}	Propagation Delay Time		Enable	Any Q	4	7.5	ns
	HIGH-to-LOW Level Output		Enable	7 tily Q	-	7.0	110
t _{PZH}	Output Enable Time		Output Control	4		0.5	
	to HIGH Level Output			Any Q	2	6.5	ns
t _{PZL}	Output Enable Time		Output Control				
	to LOW Level Output			Any Q	4	9.5	ns
t _{PHZ}	Output Disable Time		Output Control	A O	0	0.5	
1112	from HIGH Level Output			Any Q	2	6.5	ns
t _{PLZ}	Output Disable Time		Output Control				
	from LOW Level Output			Any Q	2	7.5	ns
t _{PHL}	Propagation Delay Time		Clear	A= O		0.5	
	HIGH-to-LOW Level Output		Clear	Any Q	3	8.5	ns





24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N24C

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