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November 1998

## FDR8308P

### Dual P-Channel, Logic Level, PowerTrench™ MOSFET

#### General Description

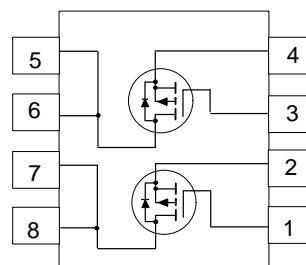
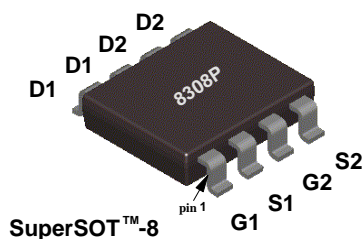
The SuperSOT-8 family of P-Channel Logic Level MOSFETs have been designed to provide a low profile, small footprint alternative to industry standard SO-8 little foot type product.

These P-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging circuits, and DC/DC conversion.

#### Features

- -3.2 A, -20 V.  $R_{DS(ON)} = 0.050 \Omega$  @  $V_{GS} = -4.5$  V,  
 $R_{DS(ON)} = 0.070 \Omega$  @  $V_{GS} = -2.5$  V.
- Low gate charge (13nC typical).
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- SuperSOT™-8 package: small footprint (40% less than SO-8); low profile(1mmthick); maximum power comparable to SO-8.



#### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDR8308P	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current - Continuous (Note 1)	-3.2	A
	- Pulsed	-20	
$P_D$	Maximum Power Dissipation (Note 1)	0.8	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	156	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted )

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = -50\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		-16		mV / $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$T_J = 55^\circ\text{C}$			-10	$\mu\text{A}$
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSS}$	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-0.9	-1.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp.Coefficient	$I_D = -50\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		2.5		mV / $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -3.2\text{ A}$		0.038	0.05	$\Omega$
		$T_J = 125^\circ\text{C}$		0.053	0.075	
		$V_{GS} = -2.5\text{ V}, I_D = -2.7\text{ A}$		0.054	0.07	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -4.5\text{ V}, I_D = -3.2\text{ A}$		13		S
DYNAMIC CHARACTERISTICS						
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1240		pF
$C_{oss}$	Output Capacitance			270		pF
$C_{rss}$	Reverse Transfer Capacitance			100		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -5\text{ V}, I_D = -1\text{ A},$		8	16	ns
$t_r$	Turn - On Rise Time	$V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		15	27	ns
$t_{D(off)}$	Turn - Off Delay Time			45	65	ns
$t_f$	Turn - Off Fall Time			30	50	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -4.5\text{ A},$		13	19	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = -4.5\text{ V}$		1.8		nC
$Q_{gd}$	Gate-Drain Charge			3		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-0.67	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.67\text{ A}$ (Note 2)		-0.7	-1.2	V

Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



156 $^\circ\text{C}/\text{W}$  on a 0.0025 in $^2$  pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

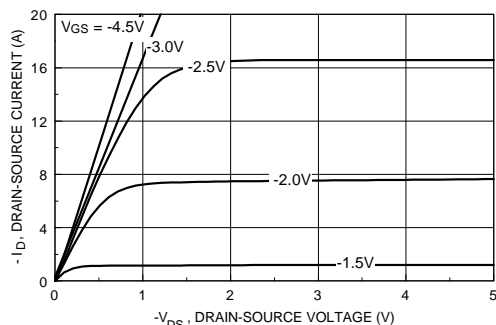


Figure 1. On-Region Characteristics.

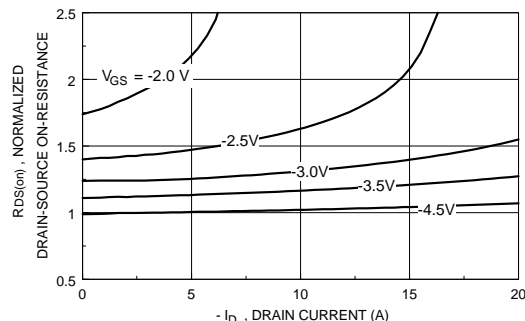


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

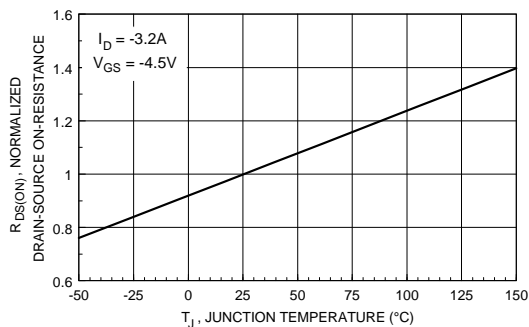


Figure 3. On-Resistance Variation with Temperature.

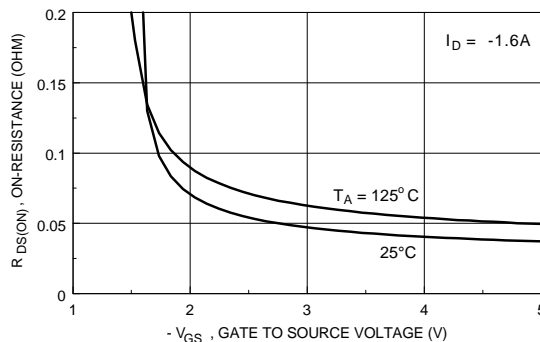


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

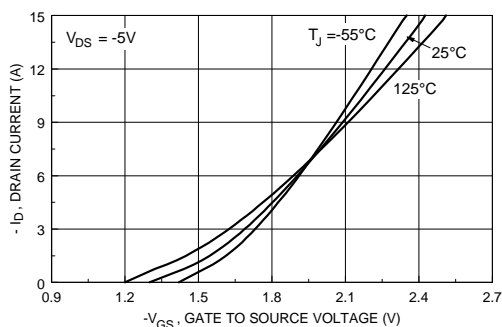


Figure 5. Transfer Characteristics.

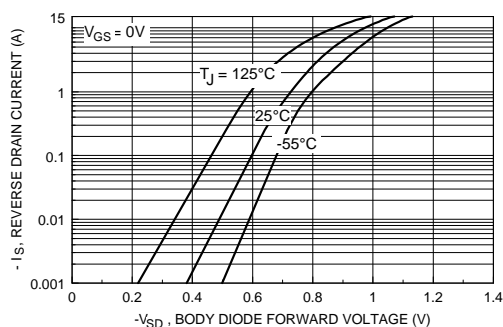


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics (continued)

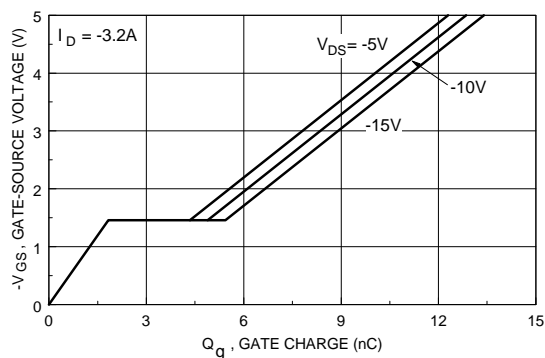


Figure 7. Gate Charge Characteristics.

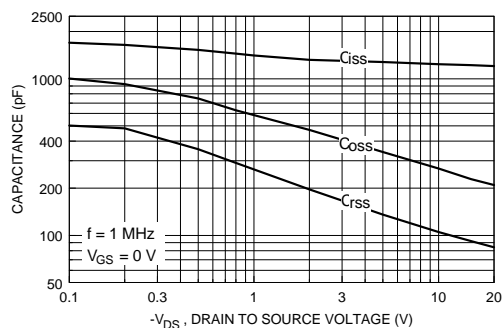


Figure 8. Capacitance Characteristics.

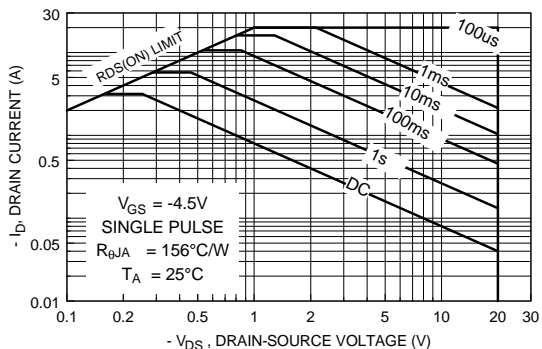


Figure 9. Maximum Safe Operating Area.

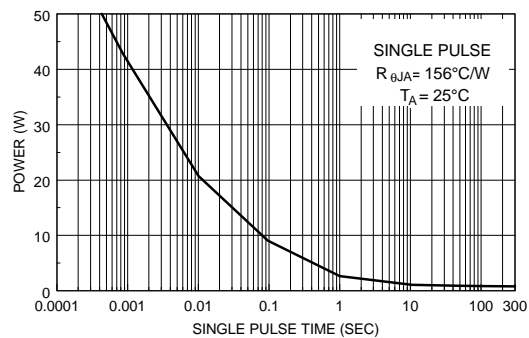


Figure 10. Single Pulse Maximum Power Dissipation.

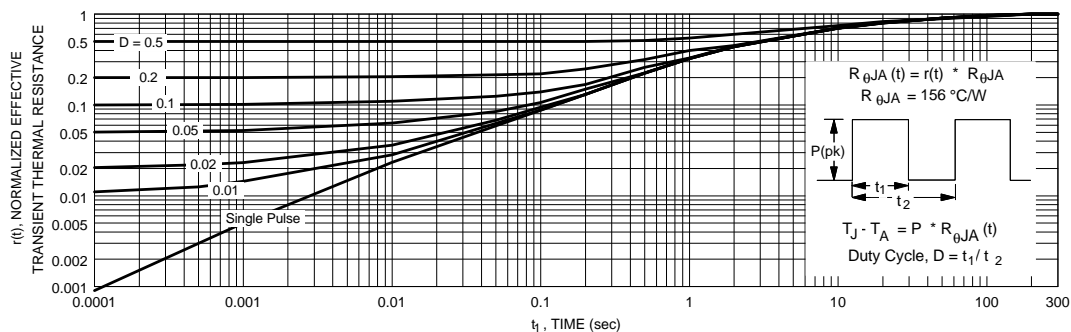


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1.  
Transient thermal response will change depending on the circuit board design.

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