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January 2000  
 Revised June 2005

## 74VCXH16373 Low Voltage 16-Bit Transparent Latch with Bushold

### General Description

The VCXH16373 contains sixteen non-inverting latches with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear to be transparent to the data when the Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH, the outputs are in a high impedance state.

The VCXH16373 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74VCXH16373 is designed for low voltage (1.2V to 3.6V)  $V_{CC}$  applications with output compatibility up to 3.6V.

The 74VCXH16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

### Features

- 1.2V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminates the need for external pull-up/pull-down resistors
- $t_{PD}$  ( $I_n$  to  $O_n$ )  
 3.0 ns max for 3.0V to 3.6V  $V_{CC}$
- Static Drive ( $I_{OH}/I_{OL}$ )  
 $\pm 24$  mA @ 3.0V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:  
 Human body model > 2000V  
 Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

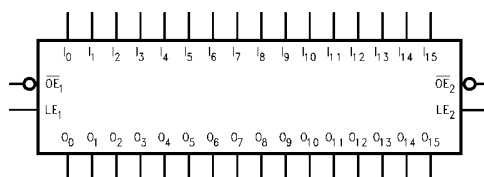
### Ordering Code:

Order Number	Package Number	Package Description
74VCXH16373G (Note 1)(Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74VCXH16373MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

**Note 1:** Ordering Code "G" indicates Tray.

**Note 2:** Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

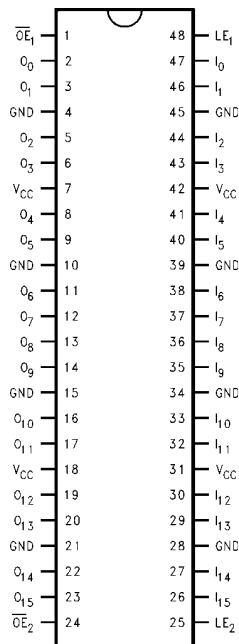
### Logic Symbol



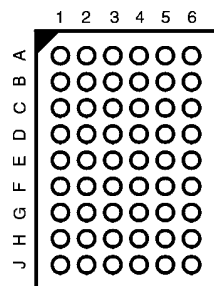
74VCXH16373

### Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$LE_n$	Latch Enable Input
$I_0-I_{15}$	Bushold Inputs
$O_0-O_{15}$	Outputs
NC	No Connect

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	$O_0$	NC	$\overline{OE}_1$	$LE_1$	NC	$I_0$
<b>B</b>	$O_2$	$O_1$	NC	NC	$I_1$	$I_2$
<b>C</b>	$O_4$	$O_3$	$V_{CC}$	$V_{CC}$	$I_3$	$I_4$
<b>D</b>	$O_6$	$O_5$	GND	GND	$I_5$	$I_6$
<b>E</b>	$O_8$	$O_7$	GND	GND	$I_7$	$I_8$
<b>F</b>	$O_{10}$	$O_9$	GND	GND	$I_9$	$I_{10}$
<b>G</b>	$O_{12}$	$O_{11}$	$V_{CC}$	$V_{CC}$	$I_{11}$	$I_{12}$
<b>H</b>	$O_{14}$	$O_{13}$	NC	NC	$I_{13}$	$I_{14}$
<b>J</b>	$O_{15}$	NC	$\overline{OE}_2$	$LE_2$	NC	$I_{15}$

### Truth Tables

Inputs			Outputs
$LE_1$	$\overline{OE}_1$	$I_0-I_7$	$O_0-O_7$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

Inputs			Outputs
$LE_2$	$\overline{OE}_2$	$I_8-I_{15}$	$O_8-O_{15}$
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	$O_0$

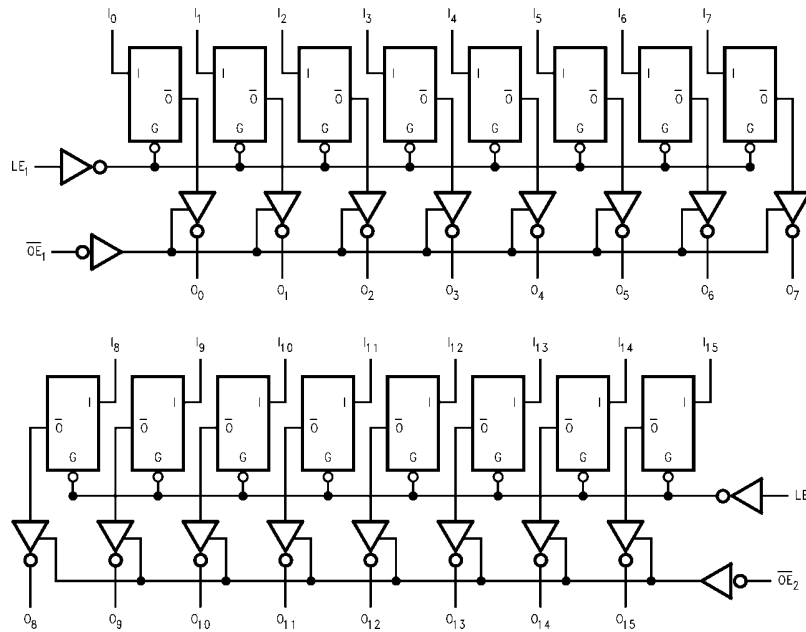
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, control inputs may not float)  
 Z = High Impedance  
 $O_0$  = Previous  $O_0$  before HIGH-to-LOW of Latch Enable

### Functional Description

The 74VCXH16373 contains sixteen edge D-type latches with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable ( $LE_n$ ) input is HIGH, data on the  $I_n$  enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time

its I input changes. When  $LE_n$  is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition on  $LE_n$ . The 3-STATE outputs are controlled by the Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW the standard outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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### Absolute Maximum Ratings (Note 3)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V
Output Voltage ( $V_O$ )	
Outputs 3-STATEd	-0.5V to +4.6V
Outputs Active (Note 4)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

### Recommended Operating Conditions (Note 5)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage ( $V_O$ )	
Output in Active States	0V to $V_{CC}$
Output in "OFF" State	0V to 3.6V
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	$\pm 24$ mA
$V_{CC} = 2.3V$ to 2.7V	$\pm 18$ mA
$V_{CC} = 1.65V$ to 2.3V	$\pm 6$ mA
$V_{CC} = 1.4V$ to 1.6V	$\pm 2$ mA
$V_{CC} = 1.2V$	$\pm 100$ $\mu$ A
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 3:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 4:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 5:** Floating or unused inputs must be held HIGH or LOW.

### DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
			1.2	$0.65 \times V_{CC}$		
$V_{IL}$	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
			1.2		$0.05 \times V_{CC}$	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12$ mA $I_{OH} = -18$ mA $I_{OH} = -24$ mA	2.7 - 3.6	$V_{CC} - 0.2$		V
			2.7	2.2		
			3.0	2.4		
			3.0	2.2		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA $I_{OH} = -12$ mA $I_{OH} = -18$ mA	2.3 - 2.7	$V_{CC} - 0.2$		
			2.3	2.0		
			2.3	1.8		
			2.3	1.7		
		$I_{OH} = -100 \mu A$ $I_{OH} = -6$ mA	1.65 - 2.3	$V_{CC} - 0.2$		
			1.65	1.25		
		$I_{OH} = -100 \mu A$ $I_{OH} = -2$ mA	1.4 - 1.6	$V_{CC} - 0.2$		
			1.4	1.05		
		$I_{OH} = -100 \mu A$	1.2	$V_{CC} - 0.2$		

DC Electrical Characteristics (Continued)							
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units	
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7 – 3.6		0.2	V	
		I <sub>OL</sub> = 12 mA	2.7		0.4		
		I <sub>OL</sub> = 18 mA	3.0		0.4		
		I <sub>OL</sub> = 24 mA	3.0		0.55		
		I <sub>OL</sub> = 100 μA	2.3 – 2.7		0.2		
		I <sub>OL</sub> = 12 mA	2.3		0.4		
		I <sub>OL</sub> = 18 mA	2.3		0.6		
		I <sub>OL</sub> = 100 μA	1.65 – 2.3		0.2		
I <sub>I</sub>	Input Leakage Current	Control Pins	0 ≤ V <sub>I</sub> ≤ 3.6V	1.4 – 3.6		±5.0	μA
		Data Pins	V <sub>I</sub> = V <sub>CC</sub> or GND	1.4 – 3.6		±5.0	μA
I <sub>I(HOLD)</sub>	Bushold Input Minimum Drive Hold Current	V <sub>IN</sub> = 0.8V	3.0		75.0	μA	
		V <sub>IN</sub> = 2.0V	3.0		-75.0		
		V <sub>IN</sub> = 0.7V	2.3		45.0		
		V <sub>IN</sub> = 1.6V	2.3		-45.0		
		V <sub>IN</sub> = 0.57V	1.65		25.0		
I <sub>I(OD)</sub>	Bushold Input Over-Drive Current to Change State	(Note 6)	3.6		450	μA	
		(Note 7)	3.6		-450		
		(Note 6)	2.7		300		
		(Note 7)	2.7		-300		
		(Note 6)	1.95		200		
I <sub>OZ</sub>	3-STATE Output Leakage	0 ≤ V <sub>O</sub> ≤ 3.6V	1.2 – 3.6			±10.0	μA
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
I <sub>OFF</sub>	Power-OFF Leakage Current	0 ≤ (V <sub>O</sub> ) ≤ 3.6V	0		10.0	μA	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	1.2 – 3.6		20.0	μA	
		V <sub>CC</sub> ≤ (V <sub>O</sub> ) ≤ 3.6V (Note 8)	1.2 – 3.6		±20.0		
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.7 – 3.6		750	μA	

**Note 6:** An external driver must source at least the specified current to switch from LOW-to-HIGH.  
**Note 7:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.  
**Note 8:** Outputs disabled or 3-STATE only.

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AC Electrical Characteristics (Note 9)							
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Figure Number
				Min	Max		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay LE to O <sub>n</sub>	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.0	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.9		
			1.8 ± 0.15	1.5	7.8		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1	1.0	15.6		Figures 7, 8
			1.2	1.5	39.0		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to O <sub>n</sub>	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.0	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.4		
			1.8 ± 0.15	1.5	6.8		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1	1.0	13.6		Figures 7, 8
			1.2	1.5	34.0		
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.6		
			1.8 ± 0.15	1.5	9.2		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1	1.0	18.4		Figures 7, 9, 10
			1.2	1.5	46.0		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	3.8		
			1.8 ± 0.15	1.5	6.8		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1	1.0	13.6		Figures 7, 9, 10
			1.2	1.5	34.0		
t <sub>S</sub>	Setup Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 6
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	2.5			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1	3.0			Figures 6, 7
			1.2	6.0			
t <sub>H</sub>	Hold Time	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 1.0	1.0		ns	Figures 1, 6
			2.5 ± 0.2	1.0			
			1.8 ± 0.15	1.0			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1	1.2			Figures 6, 7
			1.2	3.6			
t <sub>W</sub>	Pulse Width	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	1.5		ns	Figures 1, 4
			2.5 ± 0.2	1.5			
			1.8 ± 0.15	4.0			
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1	4.0			Figures 4, 7
			1.2	8.0			
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output to Output Skew (Note 10)	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 5Ω	1.5 ± 0.1		1.5		
			1.2		1.5		

**Note 9:** For C<sub>L</sub> = 50pF, add approximately 300 ps to the AC maximum specification.

**Note 10:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

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Dynamic Switching Characteristics					
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V <sub>OHV</sub>	Quiet Output Dynamic Valley V <sub>OH</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

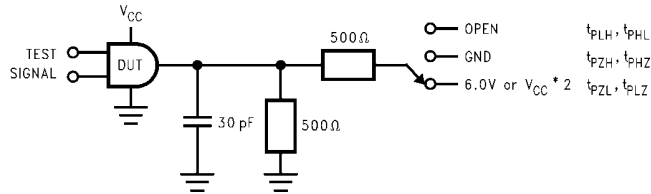
  

Capacitance					
Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C	Units	
			Typical		
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 1.8V, 2.5V or 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	6.0	pF	
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	7.0	pF	
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz, V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	20.0	pF	



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**AC Loading and Waveforms ( $V_{CC}$  3.3V  $\pm$  0.3V to 1.8V  $\pm$  0.15V)**



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$ ; $1.8V \pm 0.15V$
$t_{PZH}$ , $t_{PHZ}$	GND

FIGURE 1. AC Test Circuit

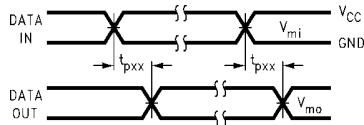


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

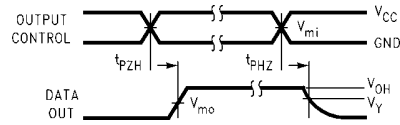


FIGURE 3. 3-STATE Output HIGH Enable and Disable Times for Low Voltage Logic

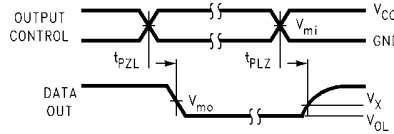


FIGURE 4. 3-STATE Output LOW Enable and Disable Times for Low Voltage Logic

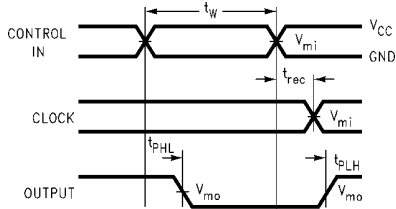


FIGURE 5. Propagation Delay, Pulse Width and  $t_{REC}$  Waveforms

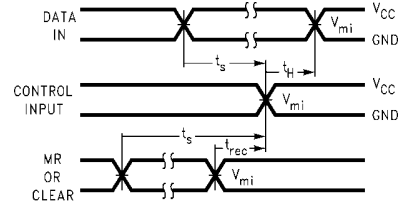
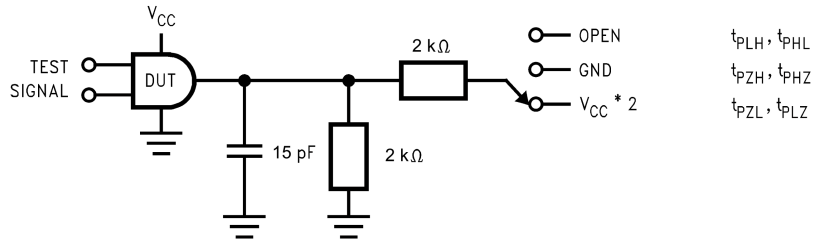


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	$V_{CC}$		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**AC Loading and Waveforms ( $V_{CC} 1.5 \pm 0.1V$  to  $1.2V$ )**



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 7. AC Test Circuit

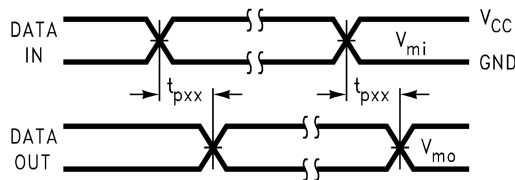


FIGURE 8. Waveform for Inverting and Non-Inverting Functions

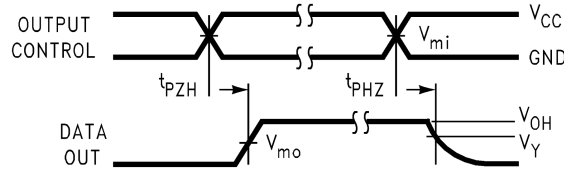


FIGURE 9. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

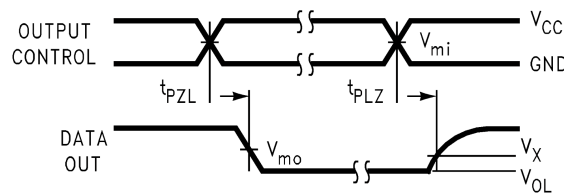
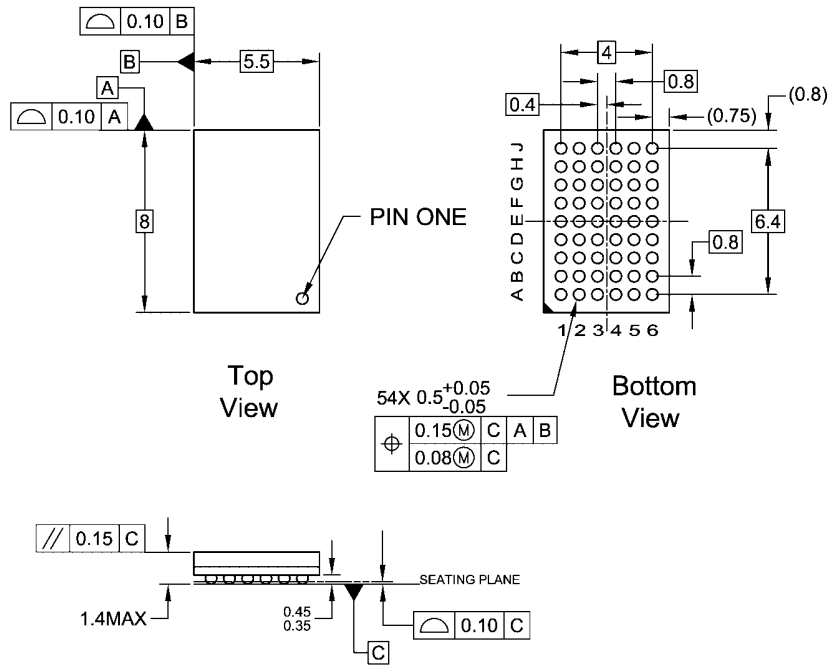


FIGURE 10. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	$V_{CC}$
	$1.5V \pm 0.1V$
$V_{mi}$	$V_{CC}/2$
$V_{mo}$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.1V$
$V_Y$	$V_{OH} - 0.1V$

74VCXH16373

**Physical Dimensions** inches (millimeters) unless otherwise noted



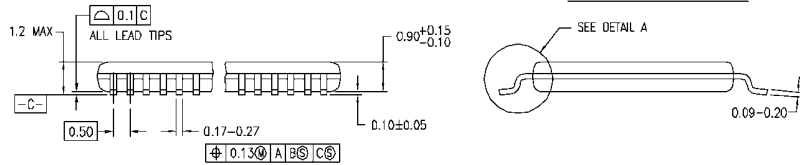
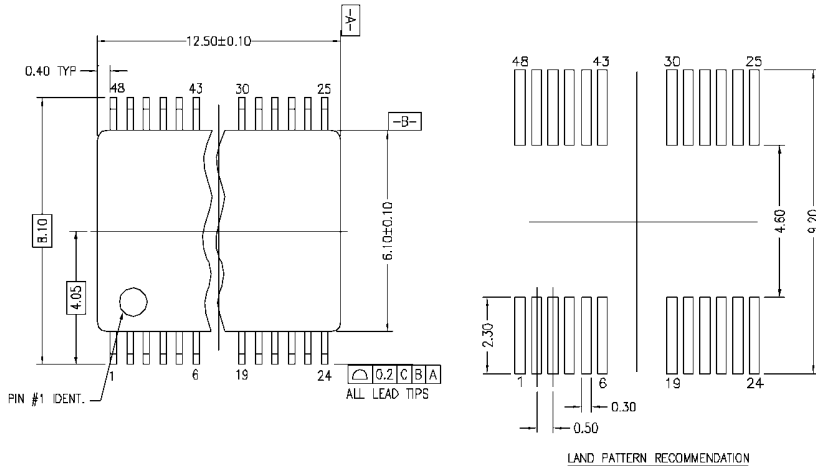
NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A  
(Preliminary)**

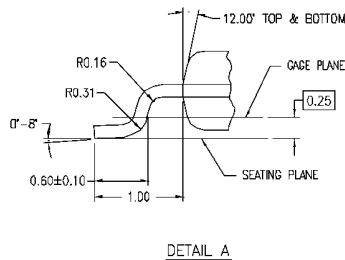
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



MTD48REVC

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
 Package Number MTD48**

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