

Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor](#)
[74ACT563SC](#)

For any questions, you can email us directly:

sales@integrated-circuit.com



74ACT563 Octal Latch with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to ACT573 but with inverted outputs
- Outputs source/sink 24mA
- ACT563 has TTL-compatible inputs

General Description

The ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

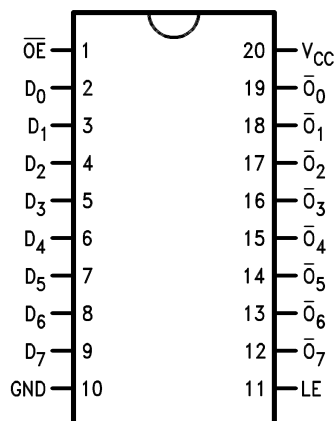
The ACT563 device is functionally identical to the ACT573, but with inverted outputs.

Ordering Information

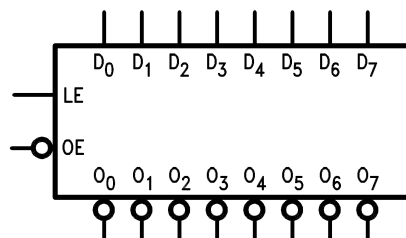
Order Number	Package Number	Package Description
74ACT563SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

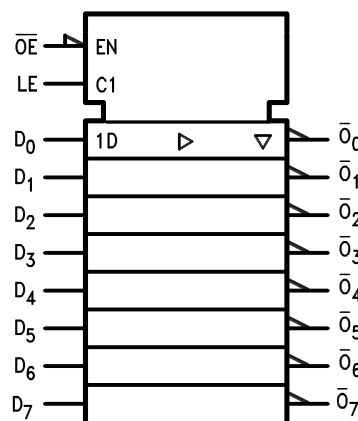
Connection Diagram



Logic Symbols



IEEE/IEC



Pin Descriptions

Pin Names	Description
D_0 – D_7	Data Inputs
LE	Latch Enable Input
\overline{OE}	3-STATE Output Enable Input
\overline{O}_0 – \overline{O}_7	3-STATE Latch Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Functional Description

The ACT563 contains eight D-type latches with 3-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Output	Function
\overline{OE}	LE	D	Q	O	
H	X	X	X	Z	High-Z
H	H	L	H	Z	High-Z
H	H	H	L	Z	High-Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level

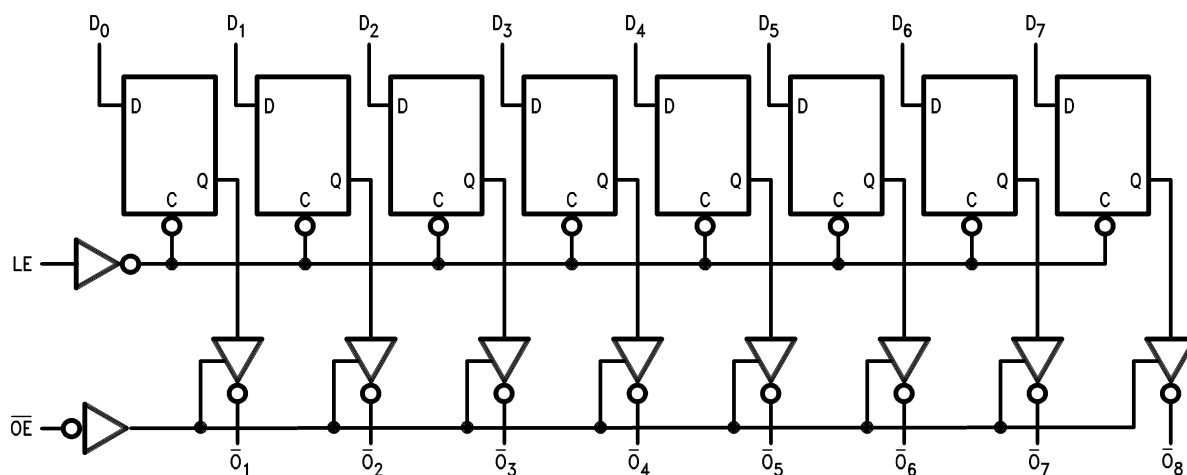
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	−20mA +20mA
V_I	DC Input Voltage	−0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	−20mA +20mA
V_O	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = −50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OH} = −24mA		3.86	3.76		
		5.5	I _{OH} = −24mA ⁽¹⁾		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA		0.36	0.44		
		5.5	I _{OL} = 24mA ⁽¹⁾		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA
I _{OZ}	Maximum 3-STATE Current	5.5	V _I = V _{IL} , V _{IH} ; V _O = V _{CC} , GND		±0.25	±2.5		μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} − 2.1V	0.6		1.5		mA
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			−75		mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		4.0	40.0		μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) ⁽³⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, D_n to \bar{O}_n	5.0	3.0	7.0	11.5	2.5	12.5	ns
t_{PHL}	Propagation Delay, D_n to \bar{O}_n	5.0	3.0	6.0	10.0	2.5	11.0	ns
t_{PLH}	Propagation Delay, LE to \bar{O}_n	5.0	3.0	6.5	10.5	2.5	11.5	ns
t_{PHL}	Propagation Delay, LE to \bar{O}_n	5.0	2.5	5.5	9.5	2.0	10.5	ns
t_{PZH}	Output Enable Time	5.0	2.5	5.5	9.0	2.0	10.0	ns
t_{PZL}	Output Enable Time	5.0	2.0	5.5	8.5	2.0	9.5	ns
t_{PHZ}	Output Disable Time	5.0	3.5	6.5	10.5	2.5	11.5	ns
t_{PLZ}	Output Disable Time	5.0	2.0	4.5	8.0	1.0	8.5	ns

Note:

3. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) ⁽⁴⁾	$T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $C_L = 50\text{pF}$	Units
			Typ.	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, D_n to LE	5.0	1.5	4.0	4.5	ns
t_H	Hold Time, HIGH or LOW, D_n to LE	5.0	-2.0	0	0	ns
t_W	LE Pulse Width, HIGH	5.0	2.0	3.0	3.0	ns

Note:

4. Voltage range 5.0 is $5.0\text{V} \pm 0.5\text{V}$.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{OPEN}$	4.5	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 5.0\text{V}$	50.0	pF

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

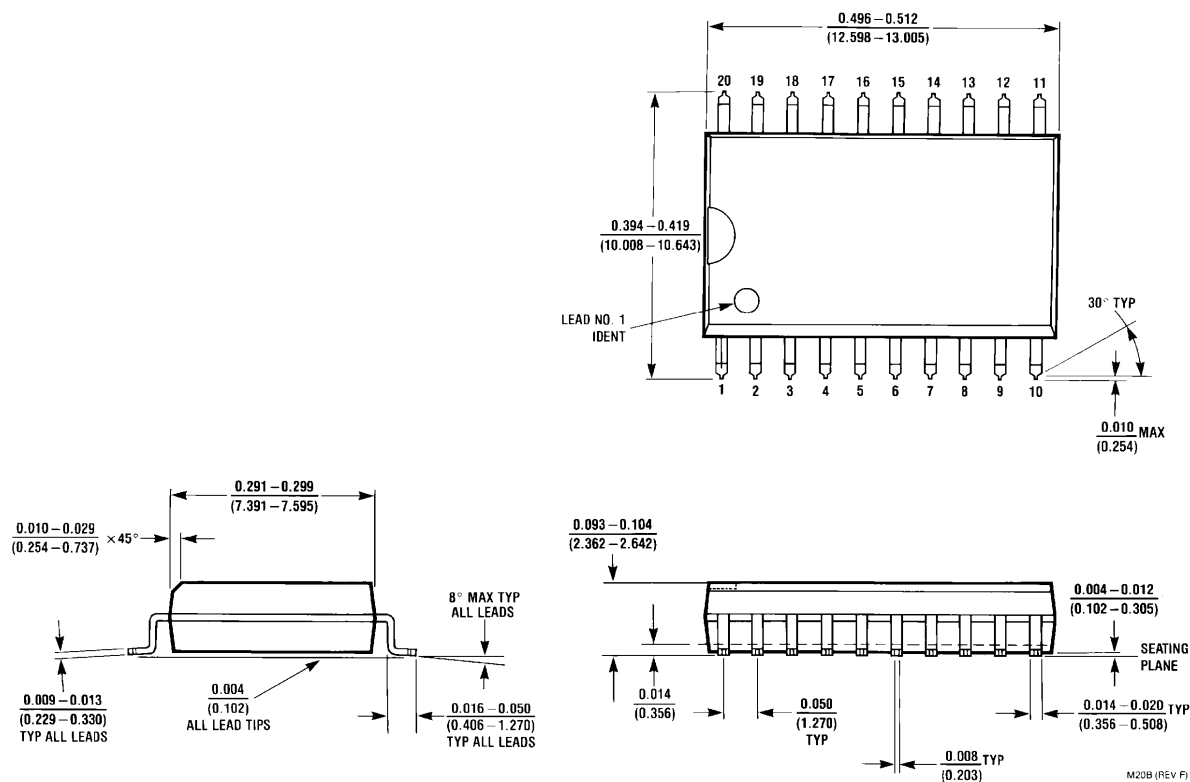



Figure 2. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE [®]	HiSeC [™]	Programmable Active Droop [™]	TinyLogic [®]
Across the board. Around the world. [™]	i-Lo [™]	QFET [®]	TINYOPTO [™]
ActiveArray [™]	ImpliedDisconnect [™]	QS [™]	TinyPower [™]
Bottomless [™]	IntelliMAX [™]	QT Optoelectronics [™]	TinyWire [™]
Build it Now [™]	ISOPLANAR [™]	Quiet Series [™]	TruTranslation [™]
CoolFET [™]	MICROCOUPLER [™]	RapidConfigure [™]	μSerDes [™]
CROSSVOLT [™]	MicroPak [™]	RapidConnect [™]	UHC [®]
CTL [™]	MICROWIRE [™]	ScalarPump [™]	UniFET [™]
Current Transfer Logic [™]	MSX [™]	SMART START [™]	VCX [™]
DOVE [™]	MSXPro [™]	SPM [®]	Wire [™]
E ² CMOS [™]	OCX [™]	STEALTH [™]	
EcoSPARK [®]	OCXPro [™]	SuperFET [™]	
EnSigna [™]	OPTOLOGIC [®]	SuperSOT [™] -3	
FACT Quiet Series [™]	OPTOPLANAR [®]	SuperSOT [™] -6	
FACT [®]	PACMAN [™]	SuperSOT [™] -8	
FAST [®]	POP [™]	SyncFET [™]	
FASTr [™]	Power220 [®]	TCM [™]	
FPS [™]	Power247 [®]	The Power Franchise [®]	
FRFET [®]	PowerEdge [™]		
GlobalOptoisolator [™]	PowerSaver [™]	TinyBoost [™]	
GTO [™]	PowerTrench [®]	TinyBuck [™]	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I24