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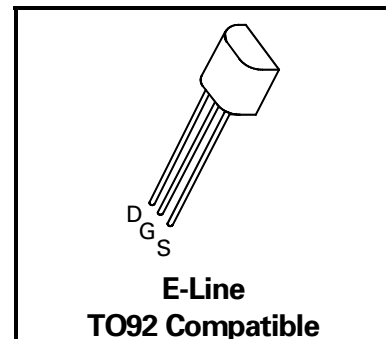
[sales@integrated-circuit.com](mailto:sales@integrated-circuit.com)

# P-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

## ZVP0120A

**ISSUE 2 – MARCH 94**
**FEATURES**

- \* 200 Volt  $V_{DS}$
- \*  $R_{DS(on)}=32\Omega$


**ABSOLUTE MAXIMUM RATINGS.**

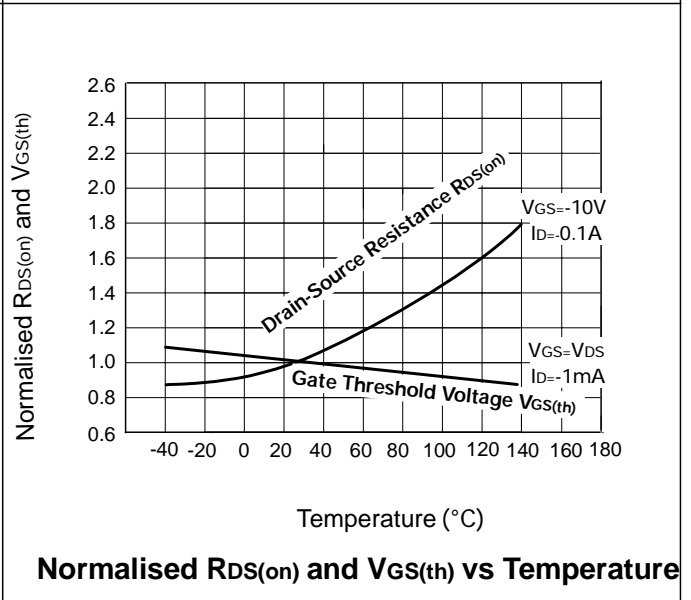
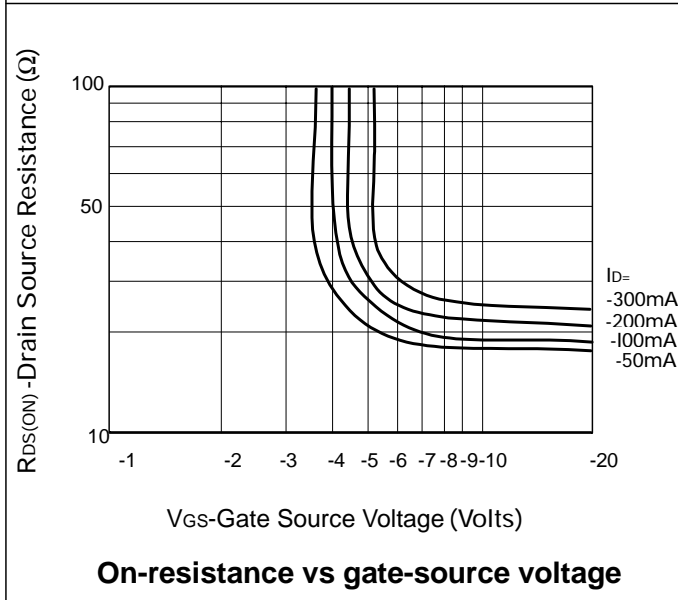
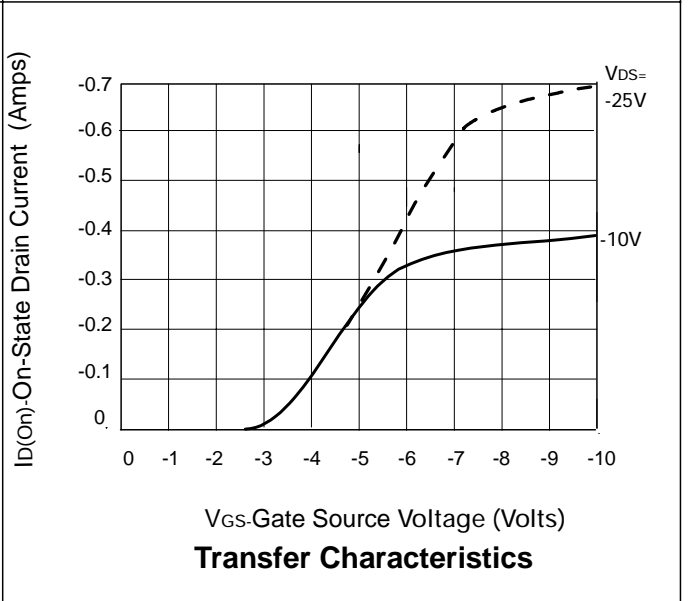
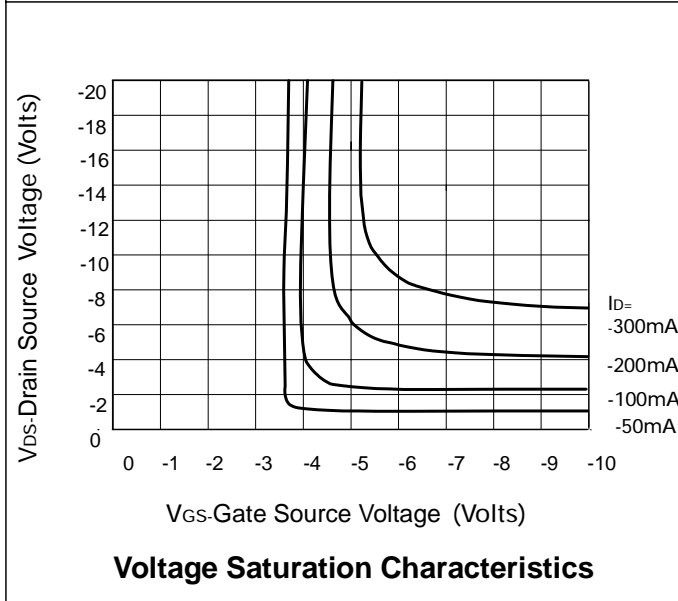
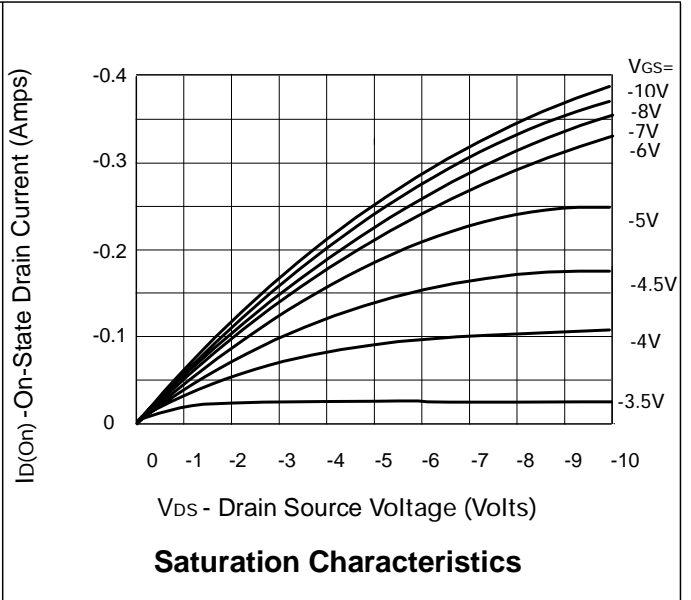
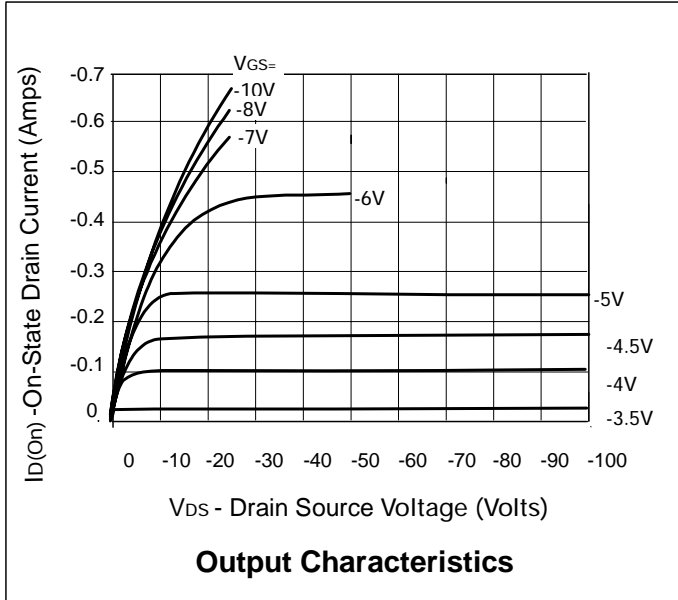
PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	$V_{DS}$	-200	V
Continuous Drain Current at $T_{amb}=25^{\circ}C$	$I_D$	-110	mA
Pulsed Drain Current	$I_{DM}$	-1	A
Gate Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation at $T_{amb}=25^{\circ}C$	$P_{tot}$	700	mW
Operating and Storage Temperature Range	$T_j; T_{stg}$	-55 to +150	$^{\circ}C$

**ELECTRICAL CHARACTERISTICS (at  $T_{amb} = 25^{\circ}C$  unless otherwise stated).**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	$BV_{DSS}$	-200		V	$I_D=-1mA, V_{GS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	-1.5	-3.5	V	$I_D=-1mA, V_{DS}=V_{GS}$
Gate-Body Leakage	$I_{GSS}$		20	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Zero Gate Voltage Drain Current	$I_{DSS}$		-10 -100	$\mu A$ $\mu A$	$V_{DS}=-200V, V_{GS}=0$ $V_{DS}=-160V, V_{GS}=0V,$ $T=125^{\circ}C(2)$
On-State Drain Current(1)	$I_{D(on)}$	-250		mA	$V_{DS}=-25V, V_{GS}=-10V$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		32	$\Omega$	$V_{GS}=-10V, I_D=-125mA$
Forward Transconductance (1)(2)	$g_{fs}$	50		mS	$V_{DS}=-25V, I_D=-125mA$
Input Capacitance (2)	$C_{iss}$		100	pF	$V_{DS}=-25V, V_{GS}=0V, f=1MHz$
Common Source Output Capacitance (2)	$C_{oss}$		25	pF	
Reverse Transfer Capacitance (2)	$C_{rss}$		7	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		7	ns	$V_{DD}\approx -25V, I_D=-125mA$
Rise Time (2)(3)	$t_r$		15	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		12	ns	
Fall Time (2)(3)	$t_f$		15	ns	

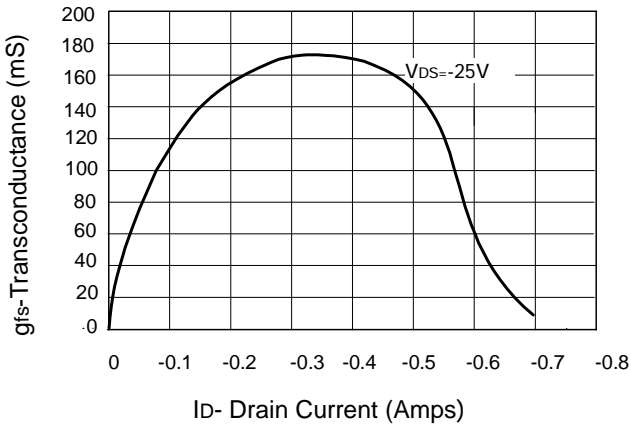
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## TYPICAL CHARACTERISTICS

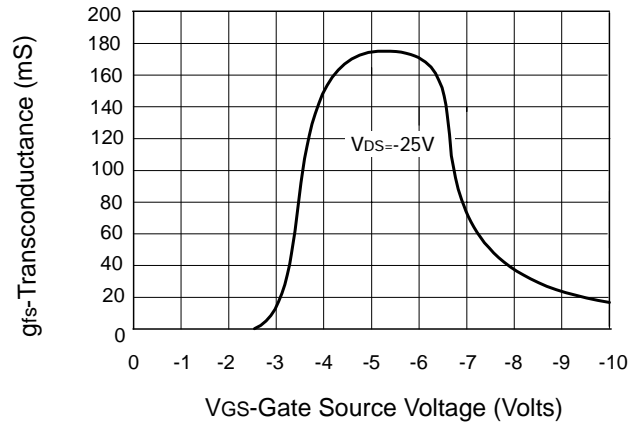


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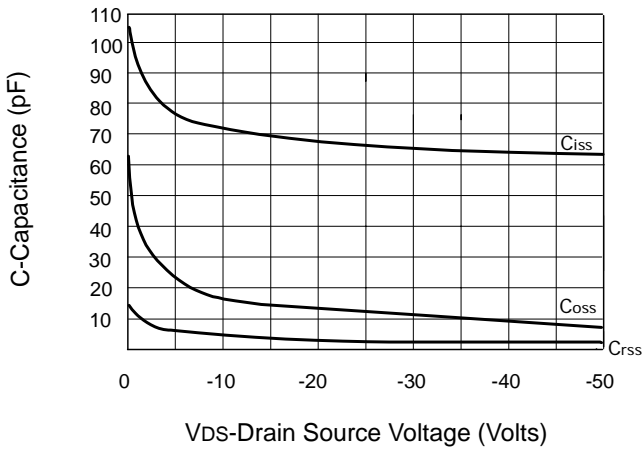
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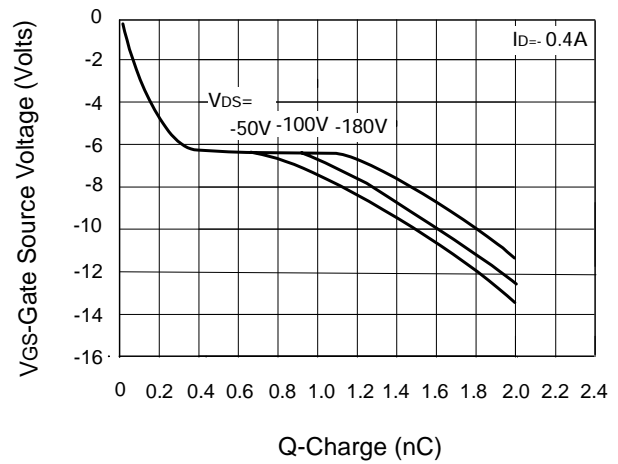
**Transconductance v drain current**



**Transconductance v gate-source voltage**



**Capacitance v drain-source voltage**



**Gate charge v gate-source voltage**